DESIGN AND IMPLEMENTATION OF HIGH-SPEED FIR FILTER USING VERILOG AND SYSTEM VERILOG FOR DSP APPLICATION

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ABSTRACT

The Finite Impulse Response (FIR) filters are widely used in Digital Signal Processing (DSP) applications due to their stability and linear phase characteristics. However, conventional FIR filter implementations suffer from high computational complexity and delay due to multiplication and addition operations. This paper presents an efficient design and implementation of an FIR filter using a Vedic Multiplier and a Parallel Prefix Adder (PPA) to enhance speed and reduce power consumption.

The Vedic multiplier, based on ancient Indian mathematics, enables faster multiplication by reducing partial product generation time. The Parallel Prefix Adder improves addition speed by minimizing carry propagation delay.

Index Terms: Finite Impulse Response (FIR) Filter, Digital Signal Processing (DSP), Parallel Prefix Adder (PPA), Kogge-Stone Adder, Vedic Multiplier, Urdhva Tiryagbhyam, High-Speed Arithmetic, Low Power Design, Verilog HDL, FPGA Implementation, VLSI Design, Signal Processing.

INTRODUCTION

Finite Impulse Response (FIR) filters are one of the most important components in Digital Signal Processing (DSP) systems. They are widely used in applications such as audio processing, image enhancement, communication systems, biomedical signal analysis (ECG), and noise reduction. FIR filters are preferred over Infinite Impulse Response (IIR) filters because they are inherently stable and can provide a linear phase response.

The performance of FIR filters mainly depends on the efficiency of arithmetic operations such as multiplication and addition. In conventional implementations, these operations introduce significant delay and power consumption, which limits the overall system performance, especially in real- time applications.

To overcome these limitations, advanced arithmetic techniques are required. Parallel Prefix Adders (PPA) are widely used for high-speed addition due to their logarithmic carry propagation delay. Among them, the Kogge-Stone Adder is one of the fastest adders, offering efficient carry computation with minimal delay. On the other hand, Vedic multipliers, based on the ancient Indian mathematical technique “Urdhva Tiryagbhyam” (vertical and crosswise), provide faster multiplication by generating partial products in parallel.

LITERATURE SURVEY

The design of high-performance FIR filters has attracted significant attention due to the increasing demand for efficient Digital Signal Processing (DSP) systems. Various techniques have been proposed to improve speed, reduce power consumption, and optimize hardware utilization.M. Pashaeifar et al. (2019) proposed a theoretical framework for evaluating the performance of DSP systems using approximate adders. Their work modeled approximation errors as additive noise and analyzed system performance using Signal-to-Noise Ratio (SNR). The study demonstrated that approximate adders can significantly reduce power consumption while maintaining acceptable accuracy levels.

Gupta et al. (2013) introduced low-power DSP architectures using approximate adders by reducing logic complexity at the transistor level. Their approach achieved substantial power savings, up to 69%, by exploiting the error tolerance of multimedia applications. However, the trade-off between accuracy and efficiency remains a key challenge.

RELATED WORK

A Several research efforts have focused on improving the performance of FIR filters by optimizing arithmetic units such as adders and multipliers.

Since multiplication and accumulation operations dominate FIR filter computations, enhancing these components significantly impacts overall system performance.

EXISTING SYSTEM

In conventional Digital Signal Processing (DSP) systems, FIR filters are typically implemented using standard arithmetic components such as array multipliers and ripple carry adders. These components perform multiplication and accumulation operations sequentially, which leads to increased propagation delay and higher power consumption.

Although these designs are simple and easy to implement, they suffer from several limitations. The ripple carry adder introduces significant delay due to sequential carry propagation, which affects the overall speed of the system. Similarly, traditional multipliers require more time for partial product generation and accumulation, resulting in slower performance.

PROPOSED SYSTEM

To overcome the limitations of conventional FIR filter designs, the proposed system introduces an optimized architecture that integrates a Parallel Prefix Adder (PPA) and a Vedic Multiplier. The main objective is to enhance speed, reduce power consumption, and improve hardware efficiency for high-performance Digital Signal Processing (DSP) applications. In this design, the multiplication operation in the FIR filter is performed using a Vedic Multiplier based on the Urdhva Tiryagbhyam (vertical and crosswise) algorithm.

SYSTEM ARCHITECTURE

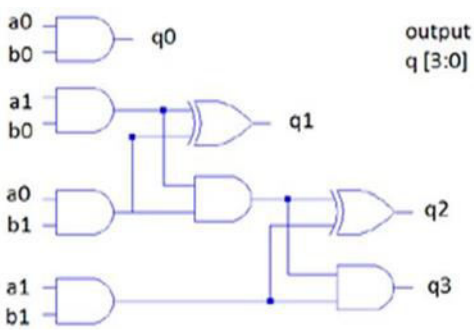

Fig 1: System Architecture

METHODOLOGY DESCRIPTION

Digital Signal Processing (DSP) applications demand efficient and high-performance filters to meet the stringent requirements of various signal processing tasks. This project presents the design and implementation of a Finite Impulse Response (FIR) filter optimized for DSP applications.

WORKING ARCHITECTURE

The Parallel Prefix Adders employ three basic stages to for the
adder operation, namely: Pre-computation of Pi and Gi, Carry generation network, post-computation.

Pre-computation stage: This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B

$Pi = Ai \oplus Bi$

$Gi = Ai . Bi$

32-bit KOGGE-STONE ADDER:

Kogge-Stone adder may be a parallel prefix type carry look ahead adder. The Kogge-Stone adder was developed by peter M. Kogge and Harold S. Stone that they printed in 1973. Kogge-Stone prefix adder may be a quick adder style

VEDIC MULTIPLIER

The Vedic Multiplier is an efficient multiplication technique derived from ancient Indian Vedic mathematics. It is based on the *Urdhva Tiryagbhyam* (Vertically and Crosswise) sutra, which enables fast and parallel computation of partial products. Due to its high speed and regular structure, it is widely used in Digital Signal Processing (DSP) and VLSI applications.

RESULTS AND DISCUSSION HOME PAGE:

The proposed FIR filter design was implemented and verified using Xilinx ISE Design Suite. The design process begins with the creation of a new project and source file, as shown in the figure above. The “New Project Wizard – Create New Source” window allows the user to define and add Verilog modules required for the FIR filter implementation.

Fig 2.1: Home Page

Using Language Templates (Verilog):

The next step in creating the new source is to add the behavioral description for counter. Use a simple counter code example from the ISE Language Templates and customize it for the counter design.

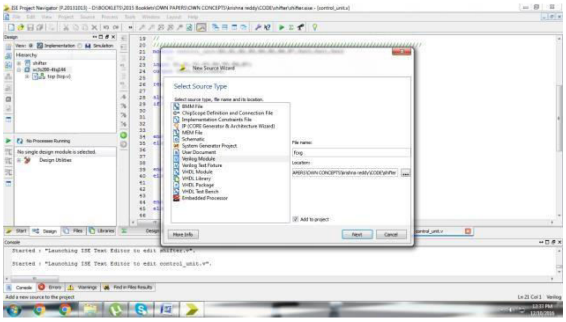

Fig 2.2: Using Verilog

MODULE DEFINITION AND PORT CONFIGURATION

In this step, a module named “counter” is created, and its ports are defined according to the required functionality. The ports include CLOCK and DIRECTION as input signals, and COUNT_OUT as the output signal. The output is defined as a bus with a range of **3:0**, indicating a 4-bit output

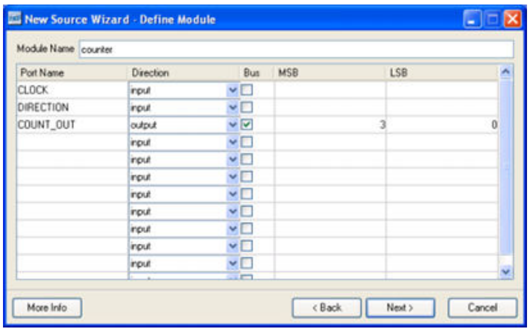

Fig 2.3: Module Definition and Port Configuration

VERILOG MODULE IMPLEMENTATION IN XILINX ISE

The Xilinx ISE interface also provides features such as source management, process execution, and error checking, which help in efficient design, simulation, and synthesis of the hardware model. This step ensures that the design is correctly implemented before moving to simulation and hardware deployment.

TIMING CONFIGURATION AND CLOCK INITIALIZATION

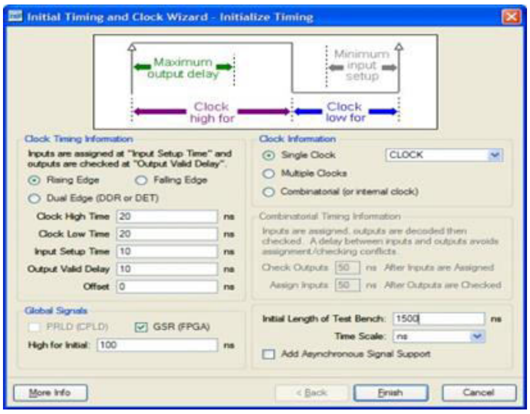

Fig 2.4: Clock Initialization

The input setup time is defined as 10 ns, which specifies the minimum time the input signal must be stable before the clock edge. Similarly, the output valid delay is set to 10 ns, indicating the time required for the output to become stable after the clock transition. The output signal

FUTURE SCOPE

Future developments may include implementing the design using advanced FPGA and ASIC technologies to achieve better performance, lower power consumption, and reduced area. The architecture can also be extended to support higher-order FIR filters, enabling more complex signal processing applications.

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COUNT_OUT is displayed as a 4-bit value (4'h0), representing the current state of the counter. Based on the applied inputs and control signals, the output remains stable throughout the simulation period.

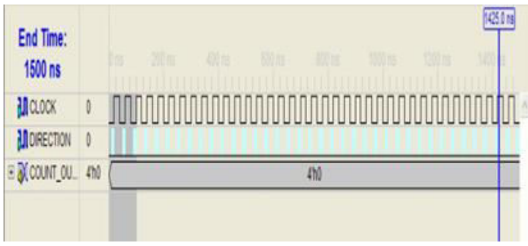

Fig 2.5: Result

CONCLUSION

The design and implementation of an FIR filter using parallel prefix adders and Vedic multipliers have demonstrated significant improvements in speed, efficiency, and resource utilization. This project highlights the potential of combining advanced arithmetic techniques to enhance digital signal processing capabilities.

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