DESIGN A SELF REPAIRABLE FAULT TOLERANT SYSTEM USING PCG

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ABSTRACT:

In this project, design a self repairable fault tolerant system using PCG (Preconditioned Conjugate Gradient) is implemented. Basically, multiplexers are key arithmetic circuits in many of these applications including digital signal processing (DSP). Initially here input is given to the flip flop block and shadow latch block. The flip flop will save the input data into two states as '0' and '1'. Shadow latch will also save the input data but it will captute the input data and present it on the data line. Flip flop will transfer the input data to perform the main operation and shadow latch will save the data in shadow memory. At last the both data will be compared using comparator and output is obtained. Hence this project reduces the errors, delay and area in effective way compared to earlier systems.

Key Words: VLSI, Digital signal processing (DSP), Multiplexer, Fault tolerant system, self repairable, PCG (Preconditioned Conjugate Gradient), Comparator.

I. INTRODUCTION

Basically all fault tolerant techniques introduce 'extra' elements into the system; 'extra' in the sense that these elements are not essential during normal operating modes. A combination of hardware, software and time redundancies termed as protective

redundancy can be incorporated in computers to bypass errors so that the final results are correct. The common approach is to employ physical redundancy to mask permanent faults and to use time redundancy to tackle transient and intermittent faults. The main objective in fault tolerant systems is to maximize reliability using minimum redundancy. By and large the research under fault tolerant systems has been addressing the logical correctness and delivery of results rather than the timeliness attribute. We are particularly interested in time redundancy techniques, since they are cost-effective as well as more suitable to applications like space missions, where there are severe constraints on space and weight. Krishna and Singh have pointed out that transient faults are especially important in applications like spacecraft circuitry which is exposed to high level of electromagnetic and elementary particle radiations, as well as in airborne computers which need to withstand transients due to lightning strikes. They assert that, "Since the entire system is in the same environment, an especially severe disturbance can result in a momentary, correlated failure of all the processors. To have the system survive transient correlated failures and still execute all its critical workload on time, designers must use time redundancy". Fault tolerance is an approach for ensuring that the system remains to be functional under anticipated or unanticipated faults covered in its fault model. This is achieved by the inclusion of an appropriate form of redundancy while designing the system. There are several aspects of fault tolerance which need to be understood and specified as part of the fault model. These include fault classification, intended post-failure functionality, type and quantity of redundancy employed, and the stages involved in fault tolerance. Issue suspicions have a critical effect. Adaptation to non-critical failure is the capacity to keep 2 14 working notwithstanding the disappointment of a restricted subset of their equipment or

programming. So the objective of the framework originator is to guarantee that the likelihood of framework disappointment is acceptably little. There can be either equipment issue or programming issue, which upsets the ongoing frameworks to fulfill their time constraints. Excess is one of techniques used to accomplish adaptation to internal failure; it very well may be dynamic, inactive or both. The dynamic replication comprises in executing similar assignment in equal on a few unmistakable processors. The inactive replication comprises in duplicating each errand on n reproductions, and just one of the n imitations executes, called essential, and the n – 1 other copy are pausing and are executed just when the essential fizzles. Progressively frameworks, adaptation to non-critical failure is given by physical, or potentially programming 49 redundancies. As we are focusing on implanted frameworks, we depend on the dispersed models which permit excess of programming parts on various processors to meet their particulars. Shortcomings can be arranged by their span as: Permanent issues, irregular deficiencies or transient flaws. Long-lasting flaws are constant, they keep on existing until the defective part is fixed or supplanted. These flaws can be brought about by disastrous framework disappointments like processor disappointments. Transient flaws emerge once and afterward disappear. For instance, an organization message doesn't arrive at its objective yet later the message is effectively retransmitted. Discontinuous shortcomings are portrayed by an issue occurring, then, at that point disappearing, then, at that point happening once more, then, at that point evaporating once more, and so forth They are hard to be characterized, however their belongings are emphatically connected. A free association is an illustration of this sort of issue. We focus on long-lasting flaws of one processor Faults are also classified with respect to their failure consequences. Omission faults occur,if

no output is delivered by the system upon failure. Value faults are those in which the output value differs from that expected or specified. Commission faults are those which make the system produce an output when it is not supposed to give any outputs. Timing faults occur when the result is not delivered at the expected time (or within a predefined4 15 Interval). A system can be classified based on its intended post-failure functionality as: Fail-operational: provides all the envisaged functions even upon failures. Fail-soft: provides a degraded service until the cause of failure disappears or is removed. Fail-safe: tries to avoid catastrophes and then abandons its functioning. Graceful degradation : continues to operate with partial degradation in functionality or performance. Fail-silent: provides correct services until a failure happens. Here the only possible failure is an omission failure and the system stops sending outputs upon failure (also known as failstop). If none of the above is specified, then the system is said to fail in an uncontrolled way (sometimes called a Byzantine failure). Redundancy for fault tolerance can be employed in several forms such as hardware, software, temporal, component, and analytical or data. In this thesis we are mainly interested in temporal and software redundancies.

FAULT TOLERANCE CLASSIFICATION

To accomplish adaptation to non-critical failure, the principal prerequisite is that transient deficiencies must be recognized.

1) TMR (Triple Modular Redundancy) Multiple duplicates are executed and mistake checking is accomplished by contrasting outcomes after fulfillment. In this plan, the overhead is consistently on the request for the quantity of duplicates running all the while.

2) PB (Primary/Backup) The undertakings are thought to be

occasional and two examples of each assignment (an essential and a reinforcement) are booked on a uni-processor framework. One of the limitations of this methodology is that the time of any undertaking ought to be a numerous of the time of its previous assignments. It likewise accepts that the execution season of the reinforcement is more limited than that of the essential. 3) PE (Primary/Exception) It is equivalent to PB technique aside from that exemption controllers are executed rather than reinforcement programs.

2. Existing method

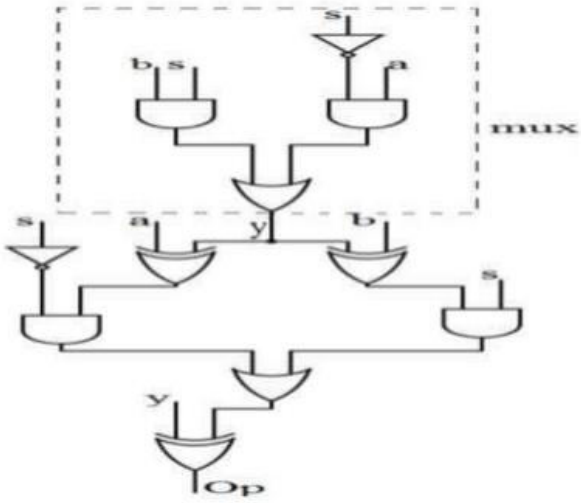

Figure 1. Existing system.

The innovation is downsizing, chip thickness is expanding so a large number of semiconductors are implanted on a solitary kick the bucket. The yield might diminish because of interaction varieties, deviation in boundaries and lithographic impacts. This high level microelectronic advancements more powerless to deficiencies. The reaction of a circuit might be invalid due to presence of deficiencies [5-8]. This prompts mistaken outcomes. Shortcoming secure frameworks are particularly expected to withstand flaws. So oneself checking and fixing is fundamental for right activity of the circuit. In self checking the shortcoming is recognized by circuit itself and in self fixing the circuit can fix itself and produces right yield. The general circuit execution relies upon individual entryways of the circuit. Utilizing modest number of entryways for configuration can build the presentation as far as deferral, region and force. To get rapid the basic way ought to be just about as least as could really be

expected. Also to get low force less number of entryways are utilized at circuit level without compromising the exactness of thecircuit. Multiplexers are utilized in wide assortment of utilizationslike adders, multipliers, correspondence, advanced sign preparing and so forth In view of the choice sign multiplexer will choose the info information and 25 passes it to the yield. The presence of issue in a multiplexer causes invalid information at the yield. The multiplexer ought to be issue secure with the goal that it gives legitimate information at the yield despite the fact that flaws are available in it. Self checking multiplexer was proposed. This self checking multiplexer planned by utilizing four transmission doors and an inverter as displayed in Fig. 1. At the point when CS is low S0N is passed to SN. Additionally when CS is high S1N is passed to SN. Accordingly it executes the capacity of multiplexer. In this self checking multiplexer when SN and SN_bar are same then it shows the presence of a shortcoming. By utilizing this construction just shortcoming is recognized and can't be repairable. To make the multiplexer self fixing two unique designs are proposed. The CS bar signal is the transformed sign of CS. In Fig. 3.1 the circuit encased in square box shows the essential construction of 2:1 multiplexer. Remaining design which is excluded from the square box is utilized for fixing the above 2:1 multiplexer. The circuit can identify all conceivable single and various deficiencies present in the 2:1 multiplexer and fixes the circuit. The circuit gives 100% mistake recuperation. Think about Fig. 3.1. Expect there is a stuck at '0' issue at y. Since y was stuck at '0', it will give consistently '0' as the yield. Anyway when this worth is passed to fixing circuit, it identifies the issue and creates right yield. This is displayed in Fig. 3.1. Essentially expect there is a stuck at '1' shortcoming at y. Since y was stuck at '1', it will give consistently '1' as the yield. Anyway when this worth is passed to fixing

circuit, it distinguishes the issue and delivers right yield. This is displayed in Fig. 3.1. So when there is issue in multiplexer block, then, at that point yield Op gives the rearranged worth of y. On the off chance that there is no issue, y esteem is passed to the yield Op. The above proposed multiplexer 1 uses extra hardware to fix. In the proposed self fixing multiplexer 2 the structure squares of multiplexer itself are self repairable.

3. PROPOSED SYSTEM

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals and and one binary digital output. A comparator circuit compares two voltages and outputs either a 1 (the voltage at the plus side; VDD in the illustration) or a 0 (the voltage at the negative side) to indicate which is larger. Comparators are often used, for example, to check whether an input has reached some predetermined value. Shadow latches are a kind of latch, sometimes out of synchronization with the other latches,sometimes software based, sometimes hardware configured. You will find this kind of circuit design in high speed digital signal processing applications. A latch circuit allows all the various connected circuits to stabilize in a state, it essentially acts as a controlmechanism to assure states are captured if other elements of the design are faster or slower.Shadow latches are a kind of latch, sometimes out of synchronization with the other latches,sometimes software based, sometimes hardware configured. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics. Flipflopsand latches are used as data storage elements. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the

other represents a "zero". Such data storage can be used for storage of state, and such a circuit is 34 described as sequential logic in electronics. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variablytimed input signals to some reference timing signal. Flip-flops can be either level-triggered (asynchronous, transparent or opaque) or edge- triggered (synchronous, or clocked). The term flip-flop has historically referred generically to both level-triggered and edge-triggered circuits that store a single bit of data using gates.Recently, some authors reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called transparent latches. Using this terminology, a level-sensitive flip-flop is called a transparent latch, whereas an edgetriggered flip-flop is simply called a flip-flop. Using either terminology, the term "flipflop" refers to a devicethat stores a single bit of data, but the term "latch" may also refer to a device that stores any number of bits of data using a single trigger. The terms "edgetriggered", and "level- triggered" may be used to avoid ambiguity.

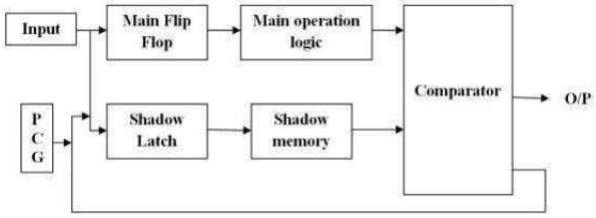

Fig.2. Proposed system

SIMULATION RESULTS

the RTL schematic of proposed system. Registertransfer logic deliberation is utilized in equipment portrayal dialects (HDLs) like Verilog and VHDL to make elevated level portrayals of a circuit, from which lower-level portrayals and at last genuine wiring can be determined. Structure at the RTL level is run of the mill practice in present day advanced plan.

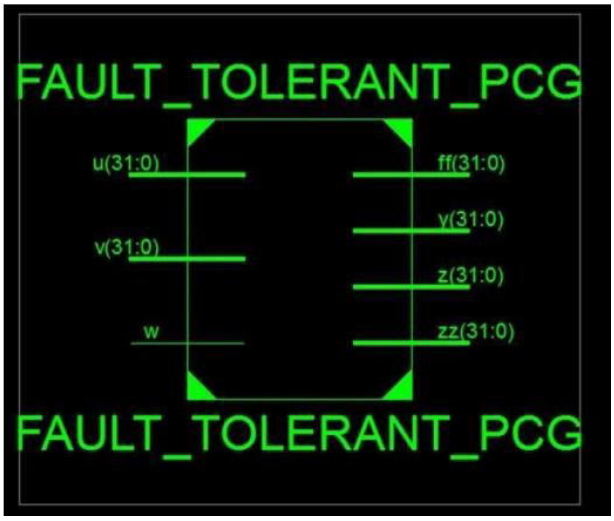

Fig.3. RTL SCHEMATIC OF PROPOSED SYSTEM.

The Technology schematic of proposed system. This schematic is generated after the optimization and technology targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized to the target Xilinx device or "technology"; for example, in terms of of LUTs, carry logic, I/O buffers, and other technology-specific components. Viewing this schematic allows you to see a technology-level representation of your HDL optimized for a specific Xilinx architecture, which might help you discover design issues early in the design process.

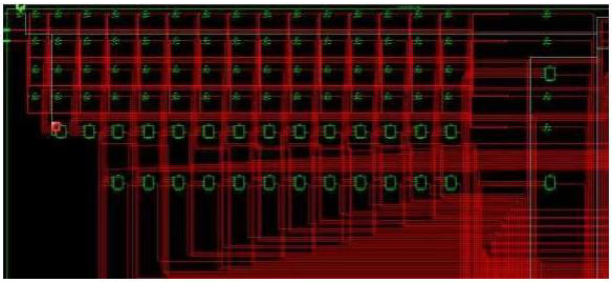

Fig.4. TECHNOLOGY SCHEMATIC OF PROPOSED SYSTEM.

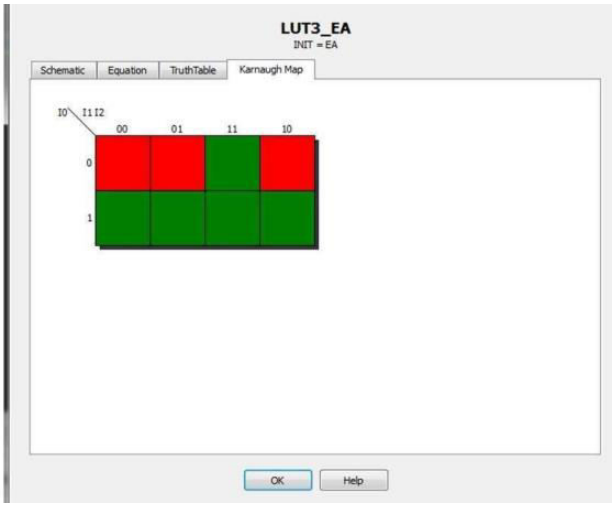

Fig.5. : K-MAP OF PROPOSED SYSTEM.

Fig.6. OUTPUT WAVEFORM OF PROPOSED SYSTEM.

V. CONCLUSION

Hence, in this project, design a self repairable fault tolerant system using PCG (Preconditioned Conjugate Gradient) is implemented. Basically, multiplexers are key arithmetic circuits in many of these applications including digital signal processing (DSP). Initially here input is given to the flip flop block and shadow latch block. Hence this project reduces the errors, delay and area in effective way compared to earlier systems.

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