DESIGNAND A ANALYSIS OF 64 BIT MAC UNIT ARCHITECTURE

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1) ABSTRACT

In computing, especially digital signal processing, the multiply–accumulate operation is a common step that computes the product of two numbers and adds that product to an accumulator. The hardware unit that performs the operation is known as a Multiplier–Accumulator (MAC unit). Design of MAC unit consists of Multiplier unit, Adder and Accumulator. This Paper focuses on review of 64-bit MAC (Multiplier and Accumulator) unit based on Vedic Mathematics using VHDL. Proposed multiplier will be design by using technique of Vedic mathematics and the rule (sutra), Urdhva Tiryakbhyam will be used for enhancing the speed of multiplier. Pipeline is one way of improving the overall processing performance of a multiplier or any processor. Here, Pipeline design will be use to increase the speed of the MAC unit, also it can perform more than one operation in a single time. Design, synthesis and simulation of 64- bit MAC unit will be done using XILINX ISE 14.5. Coding of the proposed design will be done in VHDL (Very high Speed

Integrated Circuit Hardware Description Language).

KEYWORD's: MAC, Vedic Mathematics, XILINX ISE, VHDL.

2) INTRODUCTION

Now-a-days, there is a huge demand for portable electronic products. The electronic products with low power consumption like cellular mobiles, laptops and other portable communication devices would surely lead the market trend. The MAC operation is the main computational operation in all digital designs. The speed of the processor mainly depends on the speed of the MAC unit. Development of high speed and low power MAC structure is thus very important for any real time processing application. The basic MAC structure consists of a partial product bit generation unit, a partial product bit compression unit and a final adder. Both the partial product reduction network and the accumulator unit require an addition

operation that involves a long path for carry propagation.

In the final addition operation of MAC structures, if carry propagation adder is used, the delay is increased. Since carry propagation is a time-consuming operation. To reduce this delay, a carry save adder is used instead of a carry propagation adder. But the power consumed by a carry save adder is equal to that of the carry propagation adder. MAC unit is an inevitable component in many Digital Signal Processing (DSP) applications involving multiplications and/or accumulations. MAC unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or Discrete Wavelet Transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation. Multiplication-and-accumulate operations are typical for digital filters. Therefore, the functionality of the MAC unit enables high-speed filtering and other processing typical for DSP applications. Since the MAC unit operates completely independent of the CPU, it can process data separately and thereby reduce CPU load. The application like optical communication systems which is based on DSP, require extremely fast processing of huge amount of digital data. The Fast Fourier Transform (FFT) also requires addition and multiplication. 64 bit can handle larger bits and have more memory.

Vedic Mathematics is a name which is heard many times with reference to the techniques for solving mathematics problem mentally. One of the main purposes of Vedic mathematics is to transform the tedious calculations into simpler, orally manageable operation without much help of pen and paper. Any ordinary human can perform mental operations for very small magnitude of numbers and hence Vedic mathematics provides techniques to solve operations with large magnitude of numbers easily. Vedic mathematics provides more than one method for multiplication operations. For each operation there is at least one generic method provided along with some methods which are directed towards specific cases simplifying the calculations further. Vedic mathematics provides algorithms to simplify the mathematics and hence is perfect solution for the problem stated.

After a thorough and comparative study we have found that Vedic multiplier designed by is better than other available multipliers. A MAC unit consists of a multiplier, adder and an accumulator containing the sum of the previous successive products. The MAC Unit obtain inputs from the memory location such as RAM and given to the Multiplier.MAC Unit is used in DSP Applications that uses Discrete Cosine Transform (DCT) or Discrete Wavelet Transforms (DWT). Where, Multiplication is accomplished by repetitive application of addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire Calculation. The functionality of the MAC unit enables high-speed filtering and other processing which are typical for DSP applications. Particularly, in applications like optical Communication Systems which is based on DSP, require extremely fast processing of huge amount of digital data [2].

3) LITERATURE REVIEW

Venkat pavan describes design of High Performance 64 bit MAC Unit. MAC unit performs important operation in many of the digital signal processing (DSP) applications. The multiplier is designed using modified Wallace multiplier and the adder is done with carry save adder. The total design is coded with verilog-HDL and the synthesis is done using Cadence RTL complier using typical libraries of TSMC O.18um technology. The total MAC unit operates at 217 MHz. The total power dissipation is 177.732 mW. Hence a design of high performance 64 bit Multiplier-and Accumulator (MAC) has been implemented in this paper. The total area occupied by it is 542177 11m2. Since the delay of 64 bit is less, this design can be used in the system which requires high performance in processors involving large number of bits of the operation. The MAC unit is designed using Verilog-HDL and synthesized in Cadence 180nm RTL Complier.

Sridhar describes a design and Implementation of an Efficient 64 bit MAC. MAC unit plays major role in many of the digital signal processing (DSP) applications. The MAC unit is designed with the combinations of multipliers and adders. In the proposed method MAC unit is implemented using Vedic multiplier and the adder is done with ripple carry adder. The components are reduced by implementing Vedic multiplier using the techniques of Vedic mathematics that have been modified to improve performance. a high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal

processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .The total design implemented using Xilinx. This paper presents a highly efficient optimized of MAC unit is implemented using Vedic multiplier and the adder is done with ripple carry adder. The components are reduced by implementing Vedic multiplier using the techniques of "urdhva tiryakbhyam sutra" based on Vedic mathematics is modified to improve performance. a high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .it is observed that the Vedic multiplier is much more efficient than Wallace multiplier in terms of area. An awareness of Vedic mathematics can be effectively improved if it is integrated in engineering education .

Jagadeesh presents the design of Optimized 64 Bit MAC Unit for DSP Applications. The MAC Unit has been designed with the Combinations of Multipliers and Adders. In the proposed method MAC unit is implemented using vedic multiplier and the adder is done with ripple carry adder .the components are reduced by implementing vedic multiplier using the techniques of vedic mathematics that have been modified to improve performance. A high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .the total design implemented using Xilinx. This paper presents a highly efficient optimized of mac unit is implemented using Vedic multiplier and the adder is done with ripple carry adder. The components are reduced by implementing Vedic multiplier using the techniques of "urdhva tiryakbhyam sutra" based on Vedic mathematics is modified to improve performance. A high speed processor depends significantly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. The area is optimized effectively using Vedic multiplier .it is observed that the Vedic multiplier is much more efficient than wallace multiplier in terms of area. An awareness of Vedic mathematics can be effectively improved if it is integrated in engineering education .

Harsha presents an Optimized Implementation of CSLA for 32-bit MAC using VHDL. This research work deals with the comparison of the VLSI design of

the carry select adder (CSLA) based 32-bit multiplier. Both the VLSI design of multiplier multiplies two 32-bit values and gives a product term of 64-bit values. The CLAA based multiplier uses the delay some time for performing multiplication operation where as in CSLA based multiplier also uses nearly the same delay time for multiplication operation. But the area needed for CLAA multiplier is reduced to 31 % by the CSLA based multiplier to complete the multiplication operation. With the growing importance of electronic products in day-to-day life, the need for portable electronic products with low power consumption largely increases. In this research, Multiply Accumulator unit (MAC) with carry look-ahead adder (CLA) is being designed. In the same MAC architecture design in final adder stage of partial product unit the carry save adder (CSA), carry select adder (CSLA) are also used instead of CLA to compare the power and performance. These MAC designs were simulated and synthesized using Xilinx 13.2. These multipliers are implemented using Xilinx ISE, simulation diagrams are viewed through Xilinx ISE. The simulation result shows that the MAC design with CLA has area reducing by 15%, 35% reduction is seen in power analysis and 4times increase of delay analysis. A design and performance of a DIGITAL CADENCE-based MAC both with NORMAL and REVERSIBLE was presented. HDL was used to simulate our MAC's. Digital cadence was used to synthesis the area, delay, power. Using REVERSIBLE improves the performance of the MAC's in terms of area and power.

An Area Efficient High Speed and Low Power MAC Unit. With the growing importance of electronic products in day-to-day life, the need for portable electronic products with low power consumption largely increases. In this paper, an area efficient high speed and low power Multiply Accumulator unit (MAC) with carry look-ahead adder (CLA) as final adder is being designed. In the same MAC architecture design in final adder stage of partial product unit the carry save adder (CSA), carry select adder (CSLA) and carry skip adder(CSKPA) are also used instead of CLA to compare the power and performance. These MAC designs were simulated and synthesized using Xilinx 8.1. The simulation result shows that the MAC design with CLA has area reducing by 16.7%, speed increase by 1.95% and the consumed power reducing by 0.5%. In this paper, a design of a low power MAC structure is presented. The performance of the MAC unit with adders like carry skip, carry save, carry select and carry look ahead adder are compared. The overall

power delay product and area of the MAC structure with CLA adder is found to be less than the MAC unit with the other three adders .

PARAMETERS	REF [1] Design of High Performance 64 bit MAC Unit	REF [2] Design and Implementation of an Efficient 64 bit MAC	REF [3] Design of Optimized 64 Bit MAC Unit for DSP Applications
Frequency (Mhz)	217	---	---
Power (mW)	177.732	---	175
Delay (nsec)	4.9	---	---
Cells	11916	---	---
Cell area (um^2)	542177		
No. of LUTs	---	129	129
No of SLICES	---	79	79
Total No of LUTs	---	158	158
No of IOBs	---	256	256
MULTIPLIER USED	Wallace multiplier	Vedic Multiplier	Vedic Multiplier
ADDER USED	Carry save adder	Ripple Carry Adder	Ripple Carry Adder

TABLE1.COMPARISSION BETWEEN DIFFERENT MAC UNITS

4)PROPOSED DESIGN

The Proposed work is to design of High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL. High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) can be composed with Vedic Multiplier, CSA adder, and Accumulator. Following figure shows a proposed block diagram of High Speed Efficient 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL. The proposed work is likely to achieve the Vedic Multiplier, CSA adder, and Accumulator & Multiplier-And Accumulator (MAC) based on Vedic Mathematics Using VHDL. Hence, 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic Mathematics Using VHDL with high speed will be probable outcome of this research work.

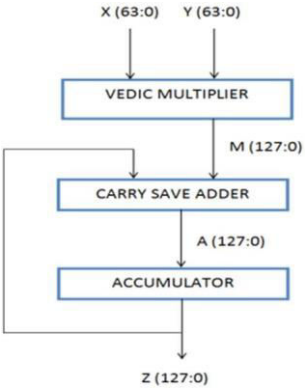

FIGURE 1: PROPOSED DIAGRAM OF 64-BIT MAC

5)CONCLUSION

In this paper we have discussed in detail about 64-bit MAC (Multiplier and Accumulator) unit based on Vedic Mathematics using VHDL. Design, synthesis and simulation of 64-bit MAC unit will be done using XILINX ISE 14.5. Coding of the proposed design will be done in VHDL. Future work is likely to achieve the design, synthesis and simulation of Vedic Multiplier, CSA adder, Accumulator and finally the Multiplier-And-Accumulator (MAC) unit based on Vedic Mathematics Using VHDL. Therefore, 64-Bit Multiplier-And-Accumulator (MAC) based on Vedic

Mathematics Using VHDL is the aim of this research work.

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