DESIGN OF LOW POWER 4 - BIT COUNTER USING DIGITAL SWITCHING CIRCUITS

[1]GADHA AYYA VENKATA PRAVEEN, [2]Dr.K. HARSHA VARDHANA REDDY
[1]PG Scholar, Dept. of ECE, Sree Rama Engineering College, Tirupati, Andhra Pradesh 517507.
[2]Associate Professor, Dept. of ECE, Sree Rama Engineering College, Tirupati, Andhra Pradesh 517507.
E-Mails: praveencrec1991@gmail.com, harssa2010@gmail.com

Abstract

To minimize the consumption of power, chip area and to enhance the battery life and performance of the system, the low power VLSI circuit is designed. Scaling design or counter is used as a key element for increasing or decreasing the values of an operator depending on its previous state. During the counting process frequency and time can be measured. The major problem in scaling circuit is the power consumption due to the power dissipation in the clock during standby mode. One-third of the total power is consumed by the clock signal in a counter. In this paper, power consumption is reduced by minimizing the number of switching activities. The power consumption in counter further reduced by reducing the power consumption in flipflops. This can be achieved by combining True Single Phase Clock Logic (TSPCL) with Self-controllable Voltage Level (SVL) technique. TSPCL performs the Flip-Flop operation at high speed with low power. SVL technique suppresses the power due to leakage current and also uses a smaller number of transistors thus the system complexity also gets reduced. The proposed design consumes 27% less power than the existing design.

Key Words: TSPCL SVL, Tanner Eda, Low Power

I. INTRODUCTION

In today's world, four elements - area, speed, delay, and power consumption – are critical in driving demand for compact handheld devices such as cell phones, laptops, palmtops, and electronic devices. Area, performance, affordability, and reliability were formerly the primary considerations of VLSI designers. In the past, reliability, cost, and performance were prioritized, and power conservation was a minor consideration. However, in recent years, power has been accorded equal weight to area and speed factors. Because of increased frequencies and chip sizes, power consumption has been a critical concern in recent years. Any VLSI circuit's performance is determined by its design architecture, which optimizes power and ensures high reliability. Power optimization of circuits at many levels is required to design any circuit with low power consumption. Power dissipation reduction is a critical design issue in VLSI circuits.

A Flip-Flop itself a circuit that gives either zero or one as a stable state of the Flip-Flop. It is widely used for storing the information. In sequential logic, Flip-Flop is used as a basic storage element. Scaling circuit is an electronic device that stores the number of times that the process or event has occurred in relation with the clock signal. It is used for counting the number of pulses coming at the input line in a specific time period. The design which consumes lesser power with maximum reliability is almost important especially when it uses clock. Thus, the power of the circuit is minimized by decreasing the dissipation of power in the clock. In Complementary Metal-Oxide Semiconductor VLSI design, the basic classification of counters is synchronous and asynchronous counter and this classification depends on clock triggering.

A scaling circuit depends on adiabatic based logic and complementary pass transistor logic is designed. But the adiabatic logic is so complex to design. True Single-Phase Clock based counter, new OR logic is used to implement the counting logic. By reducing the complex and confusing path between the Flip-Flops, the counters operating frequency can be increased. This phenomenon is followed in the TSPC based counter design.

II. EXISTING METHOD

The existing system Flip-Flop is designed using the method of True Single-Phase Clock. The main objective of using TSPCL is to perform the

operation of the required Flip-Flop that consumes minimum power and also operates with maximum speed.

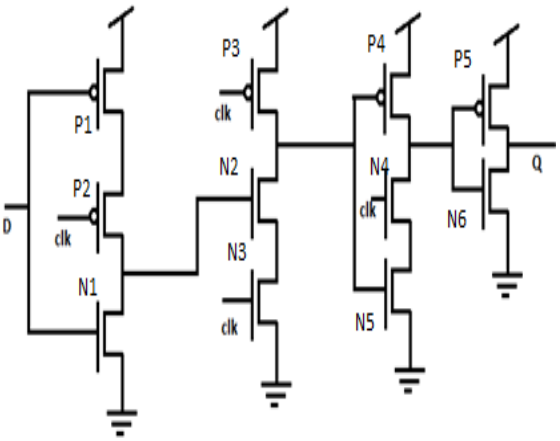


Figure – 1: D flipflop Design using TSPCL

The above figure gives the design of D Flip-Flop with TSPCL. Consider when D is 0 and CLK is low, the transistor P1 andP2 is active which in turn activates the transistor N2 of the next stage. Here P3 of this stage is active and gives 1 which is inverted and gives 0. Similarly, the given input of D gets inverted in every stage and it produces the output same as the input.

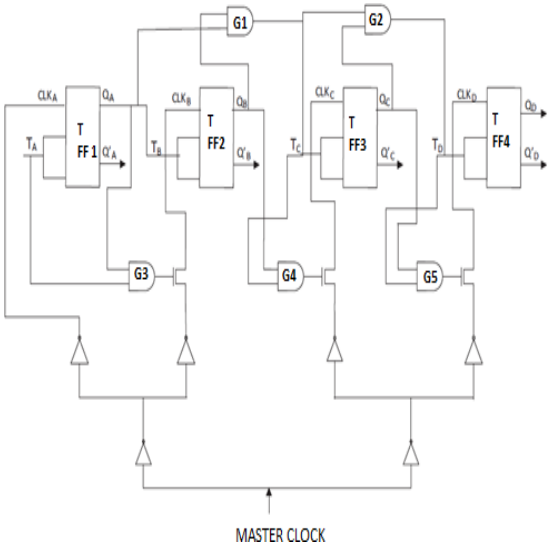
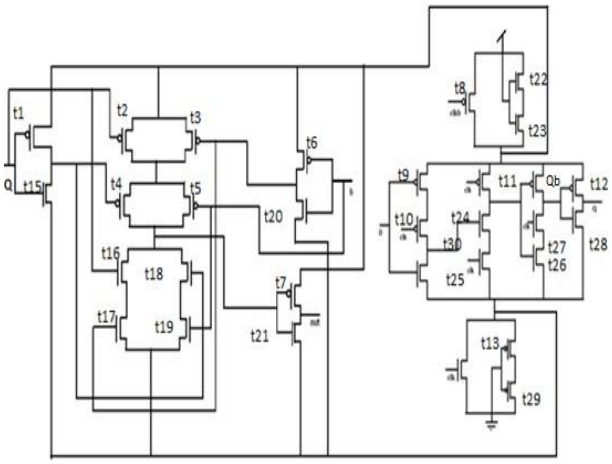


Figure – 2: Block Diagram of 4-Bit Existing Binary Up Counter

This design is applicable for wide range of bits. The Flip-Flop receives the clock signal from the clock network. This network consists of repeaters in series and eliminates clock skew. The circuit has a benefit of minimum power consumption in the clock network by introducing a combinational logic that mastery the clock based on the Flip-Flop activity. So, by avoiding the unwanted activity of clock at the inactive Flip-Flop, the power could be optimized the above Figure gives the design of 4-Bit Existing Binary Up Counter.

III. DESIGN METHODLOGY



The proposed design uses the positive edge triggered Flip-Flop. In comparison with the conventional Flip-Flop this TSPCL combined with SVL technique consumes less power.

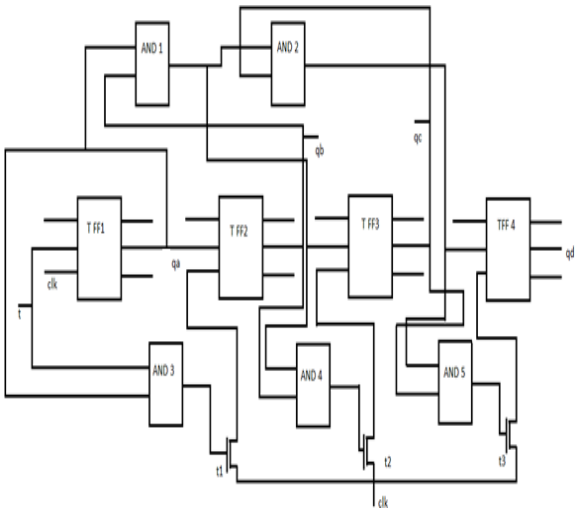
Figure - 3: Design of Proposed T Flip-Flop with Combined SVL

Figure - 3 represents the design of projected T Flip-Flop design with combined SVL. P1 is ON, N2 is ON, P2, P3 are OFF, N1 and N2 are inactive. In order to perform the normal D Flip-Flop operation, it is connected to supply and GND. When a is inactive, P1, N1, N3 are active and P2, N2 are inactive so that out becomes inactive. When a is 1, which makes P1, N3to inactive state while makes N1, N2 and P2 active state, that is out becomes one. P1, N3 are in OFF state i.e. open circuits. N1, N2 are active but as the supply voltage it gives Vdd-Vth because they act as a pull-up network.

When the NMOS transistors re connected in series it reduces the static power. P2, P3 are active but they give finite positive voltage as a replacement of GND because they act as a pull-down network. As the NMOS transistors are used in series it reduces supply voltage and also reduces leakage current during standby mode. TSPCL consists of four stages of inverter. The input gets inverted in

each stage and the final output of the TSPCL is same as that of the input. The operation of the TSPCL functions according to the clock signal.

A cascade T Flip-Flop structure is used in this system. The reason for using T Flip-Flop is it concerns for the changing activity of next state. It eliminates the clock transition when the input of T



Flip-Flop is zero. When the clock is zero it does not affect the output of the circuit and in turn maintains the previous state output whereas the output gets toggled when the clock is one. So, it is evident that the clock acts as a control signal for the counter. The block diagram of proposed counter is shown in Figure.

Figure - 4: Proposed Counter Design using modified Flip-Flop

IV. SIMULATION RESULTS

All the designs are simulated using 250nm CMOS technology library in Tanner EDA TOOL at various supply level voltages.

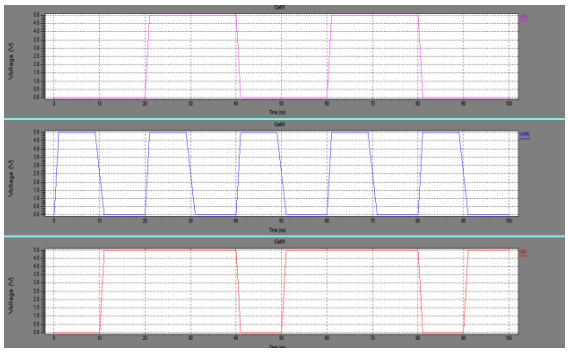


Figure - 5: Waveform of T Flip-Flop with Combined SVL

The simulation results of the proposed T Flip-Flop design using TSPCL and SVL technique is shown in Figure - 5.

The input is represented as b and the output is represented as Q and CLK as the clock input. During the first positive edge of clock, the input is 0 the output is 0 and maintains the same output till the next positive edge. In the second rising edge, the given bit is 1 so the result toggled from 0 to 1 and the output maintains for the falling edge. During the clock's third rising edge, the input is 1 so the output gets toggled from 1 to 0 and the output maintains for the clock's falling edge. In the clock signal's next rising edge, input is 1 so the output gets toggled from 0 to 1 and the output maintains for the falling edge. During the next consecutive rising edge, the input is 1 so the output gets toggled from 1 to 0 and the output maintains for the negative edge of the clock.

The simulation results of the counter using proposed T Flip-Flop is shown in Fig. 6.

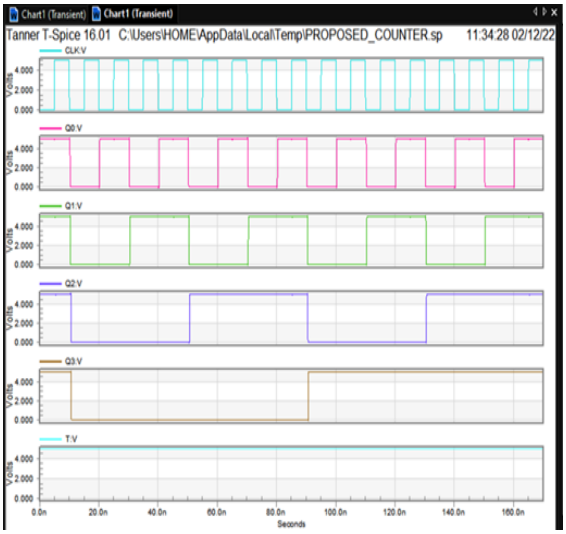


Figure – 6: Waveform of Proposed Counter

It is 4 bit up-counter which counts from zero to sixteen during the clock signal's positive edge. In the figure, qa represents the first bit, qb represents the second bit, qc represents the third bit and qd represents the fourth bit. In the simulation result waveform, it counts from zero to four.

The power dissipation of various Flip-Flop designs and counters are compared for different supply voltages. The power dissipation result for Flip-Flop design using TSPCL and SVL technique is given in

the Table - 1.

Table - 1: Power Consumption Result of Flip-Flop Design at Different Supply Voltages

FLIP- FLOP DESIGN	AVERAGE POWER CONSUMPTION IN WATTS					
	2.5V	3V	3.5V	4V	4.5V	5V
T Flip-Flop with TSPCL	0.14	0.22	0.52	0.80	0.90	1.21
T Flip-Flop with SVL	0.11	0.14	0.42	0.62	0.71	0.84
T Flip-Flop with combined SVL	0.07	0.11	0.23	0.34	0.54	0.68

From the Table - I it is shown that the power dissipation in proposed Flip-Flop is reduced by 30% for 2.5V, 19% for 3V, 44% for 3.5V, 45% for 4V, 23% for 4.5V, 18% for 5V

comparing to the existing Flip-Flop. The power dissipation result for counter design is given in the Table – 2. compares the power dissipation results of existing and proposed counter for the supply voltages ranges from 2.5Vto 5.0V.

Table -2: Power Consumption Result of 4 bit up-counterDesign at Different Supply Voltages.

COUNTER DESIGNS	AVERAGE POWER CONSUMPTION IN WATTS					
	2.5V	3V	3.5V	4V	4.5V	5V
Existing counter	3.27	3.98	4.65	5.34	6.23	6.82
Proposed counter	2.18	2.92	3.33	3.91	4.45	4.68

From the Table it is shown that the dissipation of power in proposed counter design is decreased by 33% for 2.5V, 26% for 3V, 28% for 3.5V, 26% for 4V, 28% for 4.5V, 31% for 5V comparing to the existing Flip-Flop.

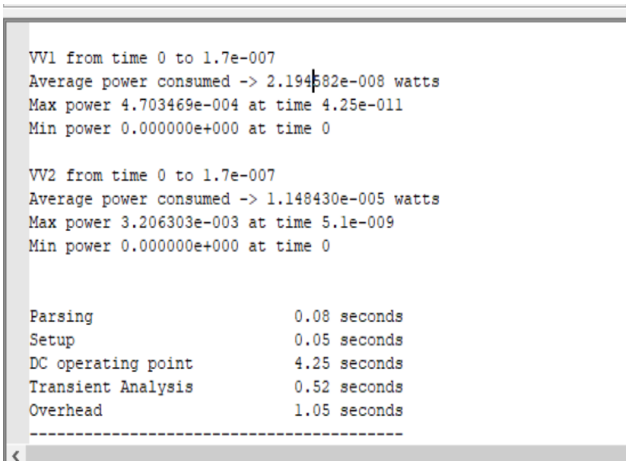


Figure – 7: Proposed power analysis

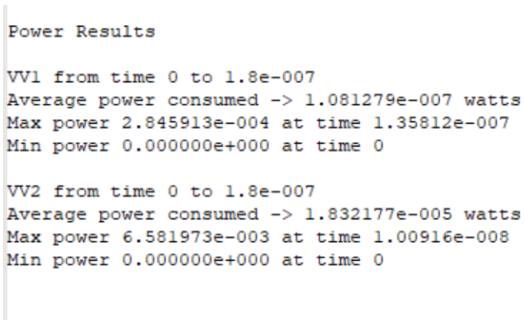


Figure – 8: Existing system power analysis

CONCLUSION

The consumption of power in the counter is minimized by using the proposed T Flip-Flop with clock gating technique. The T Flip-Flop is proposed by combining TSPCL and SVL technique. The proposed T Flip-Flop uses only 0.34 microwatt power which is 30% less than the existing T Flip- Flop design. The proposed counter design consumes 27% less power compared to the existing counter design. The projected T Flip-Flop and counter is designed and simulated using the Tanner Tool which employs 250nm CMOS technology. The proposed counter reduces power consumption and chip area which maximizes the battery life and performance of the system. Thus, it is witnessed that the combination of TSPCL, Upper and Lower SVL can be used to design the low power consuming Flip-Flop used in the construction of counters. The design is proposed only for 4 bit up-counter, the work can also be extended for the design of low power consumed wide bit counters. This project gives only the power comparison result of Flip-Flop and counter design, area analysis and delay analysis of Flip-

Flop and counter design at different Supply Voltage can also be done. Comparing to existing counter, the projected counter design utilizes 27% less power. The future work is to further minimize the power consumption of counter comparing to the proposed power of counter design.

REFERENCE

[1] Shih-Chieh Chang, Lukas P.P.P. van Ginneken, IEEE Transaction on Computers, Vol. 48, No. 9, September 1999.

[2] Oh-Hyeong Kwon, - IEEE 2003

[3] R.Uma, -Bit Fast Adder Design: Topology and Layout with Self- International Journal of Advanced Engineering Sciences and Technology, Vol No. 7, Issue No. 2, 197 205, 2011.

[4] R.Uma and Analysis on Impact of Behavioral Modeling in Performance of Synthesis Process The second International Conference on Advances in Computing and Information Technology, July 2012, Published in Advances in Intelligent Systems and Computing book series of Springer, Pg-593-602.

[5] Shrirang K. Karandikar and Sachin S. Sapatnekar , IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol. 13, No. 12, December 2005

[6] Sutherland, B. Sproull, D. Harris, Morgan Kaufmann Publisher, c1999.

[7] R.uma, Vidya Vijayan, M. Mohanapriya, Sharon Paul, Area, Delay and Power Comparison of Adder Topologies Journal of VLSI and Communication Systems, 2012.

[8] Image Processing and Pattern Recognition (SPPR 2012) May 2012, Delhi, Published in Advances in Intelligent and Soft Computing book ssing and Pattern. Pg:245-255.

[9] Mariano Aguirre-Hernandez and Monico Linares- -Adders for EnergyTransactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 4, April 2011.

[10] Pudi ,Nanotechnology, IEEE transactions on,Vol.11,Issue.1,pp.105-119,2012. Analysis and Comparison of Ripple Carry Full Adders by Speed gies and Electron Devices (EDM),2010, International Conference and Seminar on, pp.132-135,2010.