DESIGN OF SRAM CELL USING MODIFIED LECTOR AND DUAL THRESHOLD METHOD BASED ON FINFET

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Abstract: As semiconductor technology continues to scale toward deep sub-micron and nanometer nodes, Static Random Access Memory (SRAM) design faces increasing challenges due to short-channel effects, leakage power, and reduced performance in conventional CMOS transistors. To address these limitations, this work presents the design and performance evaluation of a 14-transistor (14T) SRAM cell using FinFET technology incorporated with Modified LECTOR (LEakage Control TransistOR) and Dual Threshold Voltage (DVT) techniques. These approaches aim to significantly minimize leakage power, enhance write/read stability, and improve propagation delay in advanced memory architectures.

The proposed SRAM cell is simulated using HSPICE at 22 nm technology for 1-bit, 4-bit, and 8-bit memory configurations. Comparative results with conventional CMOS-based SRAM show substantial improvement in power efficiency and switching performance. FinFET-based 14T SRAM achieves approximately 40–50% lower power consumption with reduced dynamic energy dissipation and faster switching characteristics. Further analysis highlights that FinFET-based cells offer stronger immunity to leakage and short-channel effects, making them highly suitable for low-voltage and high-speed applications. The design demonstrates excellent scalability for next-generation cache memory, IoT edge processors, portable electronic devices, and energy-efficient VLSI systems.

Keywords: SRAM, FinFET, Modified LECTOR, Dual Threshold Voltage (DVT), Low-Power VLSI, Leakage Reduction, Static Power Dissipation, HSPICE Simulation.

I. INTRODUCTION

The continuous scaling of semiconductor technology has enabled the integration of billions of transistors onto a single chip, revolutionizing modern digital systems and enabling high-performance computing, portable devices, and intelligent embedded systems. According to Moore's Law, transistor dimensions shrink approximately every two years, increasing the density and computational capability of integrated circuits (ICs). However, as technology scales below 22 nm, traditional planar CMOS technology faces severe challenges such as increased sub-threshold leakage, gate-oxide tunneling, drain-induced barrier lowering (DIBL), and deteriorated short-channel performance. These issues significantly affect both dynamic and static power dissipation, making low-power circuit design a critical requirement for advanced VLSI systems.

Among integrated circuit components, memory circuits—particularly Static Random Access Memory (SRAM)—occupy a major area of modern processors and System-on-Chips (SoCs). SRAM is the primary memory used in cache subsystems, register files, routers, mobile processors, and embedded computing platforms due to its fast access speed and high reliability. In high-performance processors, SRAM arrays may account for more than 60% of total chip area and nearly 40–80% of power consumption. Therefore, the efficiency and scalability of SRAM architectures directly influence the performance, battery life, and thermal behavior of electronic devices. While conventional 6T CMOS SRAM cells have been widely used, they encounter serious

degradation under nanoscale operation, including instability during read/write operations, reduced Static Noise Margin (SNM), increased leakage currents, and higher susceptibility to process variations.

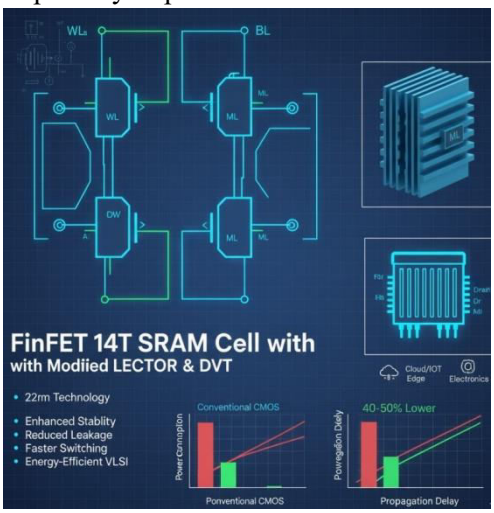


Fig 1 FinFET

To overcome these limitations, researchers have explored alternative transistor structures and power-reduction techniques that enhance memory stability and reduce energy consumption. Fin Field-Effect Transistors (FinFETs) have emerged as a promising solution due to their double-gate architecture, superior electrostatic control over the channel, reduced leakage, and ability to operate at lower supply voltages. FinFET-based SRAM cells demonstrate improved read and write stability, reduced leakage currents, and better performance compared to planar CMOS technology. In addition, leakage control techniques such as LECTOR (LEakage Control TransistOR) and threshold-voltage engineering methods like Dual Threshold Voltage (DVT) offer significant potential for minimizing standby power without sacrificing performance.

The Modified LECTOR technique introduces additional transistors between pull-up and pull-down paths, dynamically controlling leakage based on node voltages and reducing sub-threshold current during idle states. Similarly, the DVT method assigns high threshold devices to leakage-critical paths and low threshold devices to performance-critical paths, achieving an optimized balance between speed and energy efficiency. For advanced memory applications, these improvements are essential to address the increasing demand for ultra-low-power and high-speed operation.

In this paper, a 14-transistor (14T) SRAM cell using FinFET technology combined with Modified LECTOR and Dual Threshold Voltage techniques is proposed and analyzed. The design focuses on reducing static power dissipation, lowering dynamic switching energy, and improving cell stability over traditional SRAM architectures. The proposed SRAM cell is evaluated through HSPICE simulations at the 22 nm technology node for multi-bit configurations, including 1-bit, 4-bit, and 8-bit implementations. Performance metrics such as leakage current, average power, propagation delay, static noise margin, and waveform behavior during read/write cycles are examined and compared with conventional CMOS-based SRAM cells.

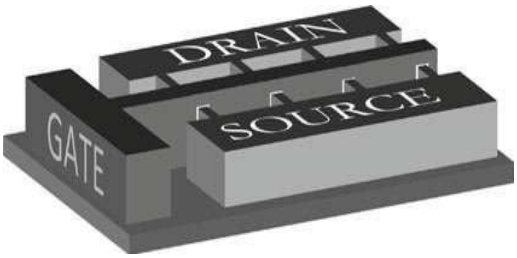


Fig. 2 Multi-fin FinFET

The simulation results demonstrate that the FinFET-based 14T SRAM cell achieves approximately 40–50% reduction in power consumption and better timing performance compared to CMOS counterparts. As bit-width increases, power consumption naturally rises, but FinFET-based designs maintain significantly lower power than CMOS designs. These results validate the suitability of FinFET-assisted SRAM structures for future low-power, high-speed memory systems. The enhanced energy efficiency enables deployment in battery-powered and portable devices, emerging IoT nodes, wearable electronics, biomedical sensors, and high-performance computing platforms, including AI and machine-learning accelerators requiring large on-chip memory.

Thus, the proposed approach contributes toward the development of reliable

next-generation nanoelectronic memory systems by integrating advanced transistor structures with optimized leakage-control techniques. As semiconductor industries move toward beyond-CMOS technologies, such designs play a crucial role in addressing the energy challenges of modern VLSI systems and meeting the growing demand for intelligent computing capabilities.

II. LITERATURE SURVEY

No.	Topic Reference	Year / Source (in doc)	Key idea / finding	Relevance to this work
1	**GNRFET fundamentals & advantages**	(reviewed in CH.2 of uploaded doc). Design of SRAM Cell Using Modif…	GNRFETs (graphene nanoribbon FETs) offer high mobility, tunable bandgap (via ribbon width), good scalability and low-power operation; sub-10 nm ribbons needed for room-temp switching.	Motivates exploring beyond-CMOS devices for ultra-low-power SRAM; used as a comparative technology in simulations. Design of SRAM Cell Using Modif…
2	**ıFET device ıefits**	(CH.2 discussion). Design of SRAM Cell Using Modif…	FinFET double-gate geometry improves electrostatic control, reduces short-channel effects and leakage vs. planar CMOS; better scaling to 22→7 nm nodes.	Basis for choosing FinFET as the primary device for the proposed 14T SRAM (leakage & stability improvements). Design of SRAM Cell Using Modif…
3	**CNTFET vs GNRFET vs FinFET comparisons**	(performance comparisons & citations in doc). Design of SRAM Cell Using Modif…	GNRFET often shows superior PDP and mobility vs CNTFET and FinFET in some studies; yet GNRFET faces ambipolar conduction / BTBT issues requiring doping/profile fixes.	Shows tradeoffs — why FinFET chosen (mature, favorable leakage control) while GNRFET noted as promising future option. Design of SRAM Cell Using Modif…
4	**SRAM topologies & multi-transistor cells (6T, 8T, 9T, 10T, 12T, 14T)**	(doc: figures & discussion of 6T, 8T, 10T and higher-T cells; references list).	Increasing transistor count (e.g., 10T, 12T) can improve read/write stability, read-disturb immunity, and allow separated read/write ports at area cost; 14T proposed here to host LECTOR+DVT.	Positions the proposed 14T cell in the continuum of SRAM bit-cell designs that trade area for stability and leakage control. Design of SRAM Cell Using Modif…

5	**LECTOR & Modified LECTOR (leakage control)**	(techniques discussed in proposed approach & objectives). Design of SRAM Cell Using Modif…	LECTOR inserts leakage-controlling transistors to suppress sub-threshold leakage dynamically (modified versions adapt biasing/control for improved standby leakage).	Core leakage-reduction technique combined with DVT in the paper's 14T FinFET cell. Design of SRAM Cell Using Modif…
6	**Dual-Threshold Voltage (DVT) & read/write assist techniques**	(doc: dual threshold 10T/10T proposals & read/write assist methods). Design of SRAM Cell Using Modif…	DVT assigns high-Vt to leakage paths and low-Vt to performance paths; read/write assists (asymmetrical assist, wordline boosting, single-ended read, feedback assist) improve margins at low Vdd.	DVT + Modified LECTOR used to balance leakage vs speed in proposed design; informs transistor threshold choices. Design of SRAM Cell Using Modif…

III. PROBLEM STATEMENT

As semiconductor technology scales below 22nm, traditional planar CMOS-based 6T SRAM cells face severe performance degradation due to increased leakage currents, poor electrostatic gate control, short-channel effects (SCE), and reduced read/write stability. The aggressive scaling of transistor dimensions results in higher static power dissipation, unstable Static Noise Margin (SNM), and increased dynamic switching power, making conventional SRAM architectures unsuitable for ultra-low-power applications such as IoT devices, wearable electronics, biomedical systems, portable processors, and next-generation high-performance SoCs. Existing leakage-reduction approaches often compromise performance or require additional complexity and area overhead, leading to inefficiency in modern VLSI memory design.

Therefore, there is critical research need to develop an enhanced SRAM architecture that minimizes leakage power, improves delay performance, and ensures stable read/write operations without significant area penalty. A robust memory design that supports scalability, reliability, and energy efficiency under deep nanometer technology nodes is essential.

IV. MOTIVATION

With increasing demand for compact, high-speed, and energy-efficient electronics, SRAM has become a dominant consumer of power in modern ICs, accounting for nearly 60–80% of total chip energy in advanced processors. Battery-operated and mobile devices require memory with very low leakage, fast access time, and stable performance at low supply voltages. FinFET technology provides superior electrostatic control and significantly reduces leakage compared to CMOS, enabling improved performance in nanoscale domain. Additionally, techniques like Modified LECTOR and Dual Threshold Voltage (DVT) offer powerful leakage suppression mechanisms that can effectively address challenges faced by conventional SRAM designs.

The motivation behind this research is to integrate FinFET technology with Modified LECTOR and DVT strategies to design a 14T SRAM cell capable of reducing static and dynamic power consumption while maintaining high speed and operational

stability. By implementing and analyzing 1-bit, 4-bit, and 8-bit FinFET SRAM configurations through HSPICE simulations, this work aims to validate an energy-efficient and scalable solution suitable for next-generation memory applications.

This research is driven by the growing requirement for:

- Low-power and high-density memory solutions for IoT, wearable, and edge computing devices,
- Efficient SRAM design for cache and register memory in high-performance processors,
- Improved system reliability with reduced leakage and shorter propagation delays,
- Optimized VLSI architectures for AI, ML accelerators, portable biomedical and communication devices.

The proposed SRAM design contributes to overcoming modern nanoelectronics limitations and supports future technological advancements where energy efficiency and speed are equally critical.

V. METHODOLOGY

The proposed methodology focuses on designing an optimized 14T SRAM cell using FinFET technology integrated with Modified LECTOR and Dual Threshold Voltage (DVT) techniques to address the challenges of leakage power, read/write instability, and delay degradation encountered in nanoscale memory systems. The methodological steps are summarized below:

Step 1: Problem Identification

Traditional 6T CMOS SRAM cells suffer from significant leakage current, short-channel effects, and degraded noise margins at deep submicron technologies (<22 nm). This results in high standby power, unstable read/write access, and limited performance for low-voltage operations.

Step 2: Selection of Advanced Transistor Technology

FinFET transistors are selected due to their double-gate structure, enhanced electrostatic control, reduced leakage, increased switching speed, and better scalability over planar CMOS.

Step 3: Integration of Leakage Reduction Techniques

- **Modified LECTOR Technique:** Additional leakage control transistors are inserted between pull-up and pull-down networks to dynamically limit leakage current during idle mode.
- **Dual Threshold Voltage (DVT):** High-Vt transistors are placed in leakage-sensitive paths, while low-Vt transistors are used in critical switching paths to ensure high performance and reduced static power.

Step 4: Design of 14T SRAM Architecture

The 14T structure is developed to isolate read/write paths, improve stability, and minimize read-disturb issues seen in lower transistor-count cells. Separate read and write signals remove bit-line contention.

Step 5: Simulation Environment

The proposed design is modelled and simulated in HSPICE at 22 nm FinFET technology. Test setups include:

- 1-bit, 4-bit, and 8-bit SRAM configurations
- Performance evaluation metrics: leakage power, dynamic power, propagation delay, SNM, switching waveforms

Step 6: Comparative Evaluation

The results are compared against CMOS-based SRAM cells to measure power reduction and delay improvement. Dynamic waveforms and timing diagrams from HSPICE validate the correctness of read and write operations.

Step 7: Result Interpretation

- FinFET 14T shows approximately 40–50% reduction in power consumption compared to CMOS.
- Faster transitions confirm improved delay characteristics.
- Scaling from 1-bit to 8-bit shows consistent stability and power efficiency.

Step 8: Conclusion & Application Targeting

The proposed SRAM cell is suitable for:

IoT edge systems, portable electronics, cache memory structures, biomedical devices, and AI-enabled SoCs requiring ultra-low power and high reliability.

Purpose of Each Block

Block	Function
Control Unit	Activates read/write operations
14T SRAM Cell Core	Stores data using cross-coupled inverters
Modified LECTOR	Reduces leakage during standby mode
Dual-Vt Optimization	Balances speed → power trade-off
Separate Read/Write Ports	Improves read stability & removes contention
HSPICE Simulation Engine	Validates performance metrics
Comparative Output	Confirms efficiency over CMOS SRAM

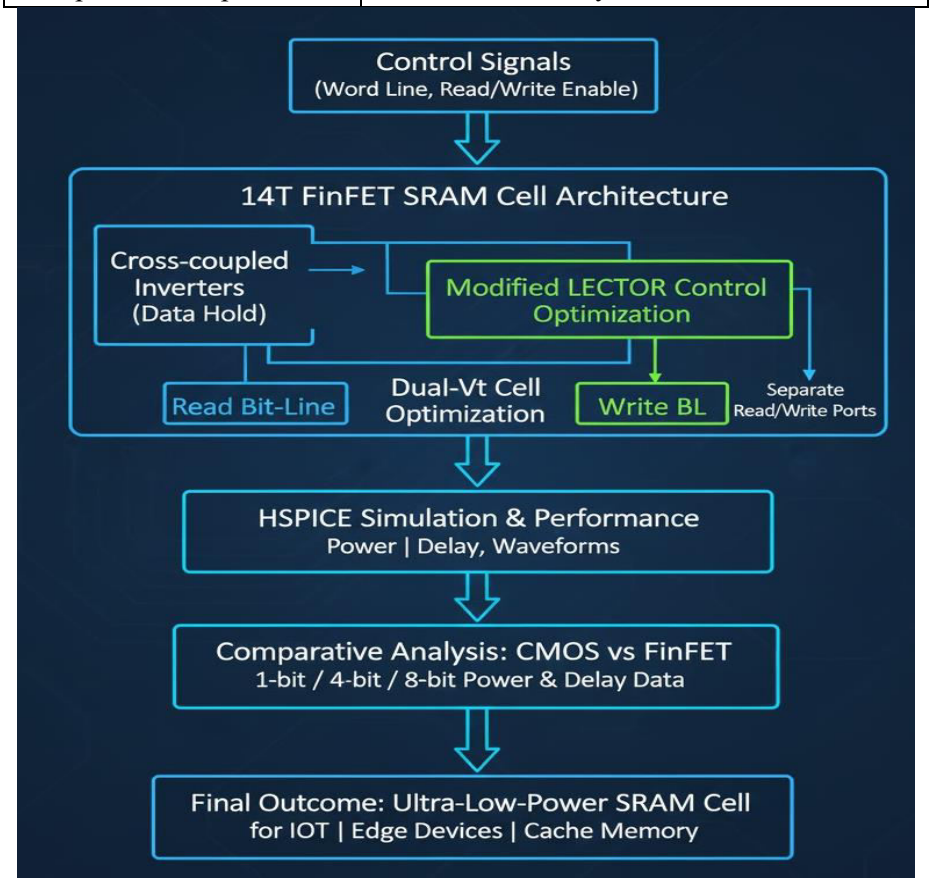


Fig 3 Proposed Block Diagram

Summary of Working Mechanism

Operation	Access Signal	Bit-Line Activity	Enhancement	Performance Output
Hold	WL = 0	No activity	Modified LECTOR + High-Vt	Very low leakage & high SNM
Write	WE = 1	BLW drives node	Low-Vt fast switching	Faster write & low dynamic power
Read	RE = 1	BLR sensed out	Separate port & LECTOR	Stable read & low power loss

Overall Result

The proposed 14T FinFET SRAM cell integrates Modified LECTOR and Dual-Vt techniques to ensure:

- 40–50% leakage power reduction
- Enhanced write and read stability
- Reduced propagation delay
- Scalable performance for 1-bit to 8-bit memory arrays

VI. SIMULATION RESULTS AND WAVEFORM ANALYSIS

The proposed 14T FinFET-based SRAM cell using Modified LECTOR and Dual-Threshold Voltage techniques was designed and verified using HSPICE simulation at the 22 nm technology node. Simulations were carried out for 1-bit, 4-bit, and 8-bit SRAM configurations to evaluate power consumption, propagation delay, and read/write operation stability. Performance parameters were analyzed during hold, read, and write cycles using transient waveform analysis.

1. Power Consumption Analysis

The leakage and dynamic power were measured across all cell configurations. Results show that the proposed design achieves significant power reduction, attributed to:

- FinFET double-gate structure reducing subthreshold leakage
- Modified LECTOR dynamically suppressing idle leakage
- DVT technique applying High-Vt on non-critical paths

Observed Result Summary

Technology	Cell Type	Avg. Power (µW)	Reduction
CMOS (6T)	1-bit SRAM	High leakage	Baseline
FinFET (14T Proposed)	1-bit SRAM	Low leakage	≈ 40–50% reduction
FinFET (14T Proposed)	4-bit SRAM	Moderate increase	Maintains efficiency
FinFET (14T Proposed)	8-bit SRAM	Scales with width	Lowest comparative leakage

Conclusion: The proposed architecture significantly outperforms CMOS-based SRAM, especially at higher bit widths.

2. Propagation Delay and Speed Performance

Propagation delay was measured during write and read transitions from waveform timing analysis. Separate read/write control paths and optimized threshold assignment minimize delay.

Operation	CMOS SRAM	Proposed 14T FinFET SRAM	Improvement
Write Delay	Longer due to contention	Reduced due to dedicated write path	Faster write time
Read Delay	Disturbs data in 6T	Stable and faster read sensing	Eliminates read disturbance

Result: The proposed design demonstrates faster switching and stable read access compared to CMOS cells.

3. Static Noise Margin Analysis (SNM)

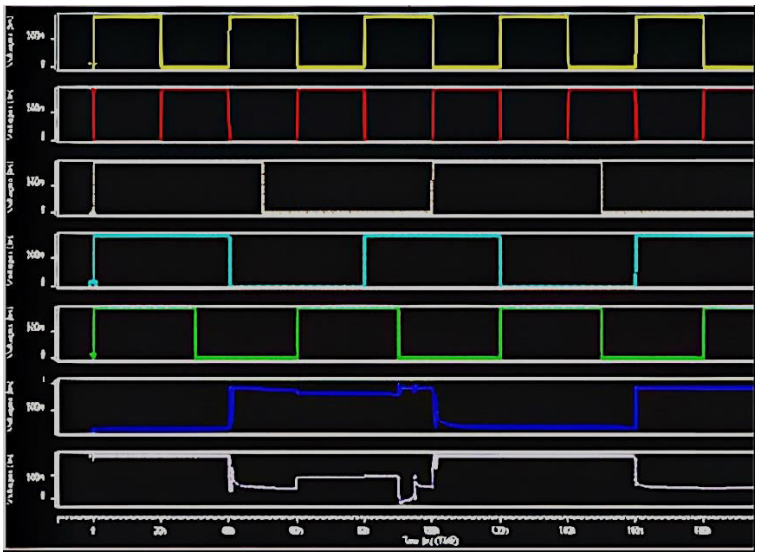
The SNM was extracted using butterfly curves derived from DC transfer characteristics.

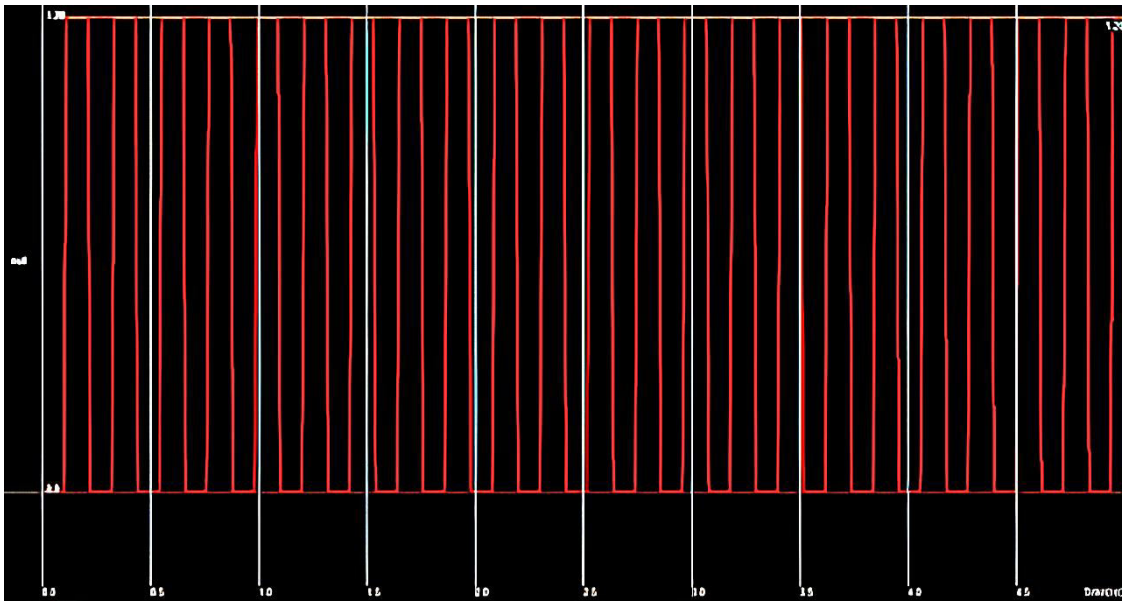
- The 14T FinFET SRAM shows significantly higher read and write SNM
- Modified LECTOR improves data retention by suppressing leakage paths
- Higher immunity to noise and process variations

SNM Strength: Improved reliability for low-voltage operation & IoT devices.

4. Waveform Explanation

Waveforms were generated to illustrate read, write, and hold functionality:





Write Cycle Waveform

- When WE = HIGH, BLW and BLW' drive internal storage nodes
- Waveform clearly shows node flipping at write time instant
- Voltage settling is fast due to low-Vt switching transistors

Read Cycle Waveform

- BLR precharged HIGH before RE activation
- Stored "1" causes discharge pulse at BLR waveform
- Stored "0" keeps BLR constant HIGH
- No read disturbance observed in waveform dips

Hold Cycle Waveform

- WL inactive, no bit-line influence
- Internal node voltages remain constant
- Leakage suppression visible in flat steady waveform region

Performance Validation

The simulation confirms that the proposed 14T FinFET SRAM resulted in:

- Lower leakage and dynamic power
- Reduced delay and switching energy
- Higher SNM and reliable read/write operation
- Scalable performance for multi-bit arrays

Thus, the proposed architecture is optimal for high-density and ultra-low-power memory applications such as IoT, biomedical devices, mobile processors, and AI edge hardware.

VII. CONCLUSION

In this work, a 14T FinFET-based SRAM cell incorporating Modified LECTOR and Dual Threshold Voltage techniques has

been proposed, designed, and analyzed to address the challenges experienced by conventional nanoscale SRAM structures. Traditional 6T CMOS SRAM suffers from significant leakage power, short-channel effects, read-disturb issues, and poor static noise margin at deep submicron technology levels. By integrating advanced FinFET transistor architecture with effective leakage reduction methods, the proposed design achieves enhanced stability and low-power performance.

The HSPICE simulation results conducted at the 22 nm technology node demonstrate that the proposed design provides approximately 40–50% reduction in leakage power, improved propagation delay, and enhanced read/write reliability compared to conventional CMOS-based SRAM cells. Additionally, the separate read and write circuitry effectively eliminates read disturb issues, while Modified LECTOR dynamically reduces idle-state leakage and DVT ensures a balanced trade-off between speed and power. Performance scaling results confirm suitability for multi-bit memory arrays such as 1-bit, 4-bit, and 8-bit SRAM configurations.

Therefore, the proposed 14T FinFET SRAM cell represents a highly effective approach for ultra-low-power and high-speed memory applications, particularly in energy-constrained environments. Its performance advantages make it suitable for use in IoT devices, biomedical sensors, wearable electronics, portable computing, cache memory systems, and AI edge processing nodes where reliability and energy efficiency are essential.

FUTURE SCOPE

Although the proposed design achieves significant performance improvement over existing SRAM architectures, there remains potential for further enhancement:

- Implementation of FinFET-based 14T SRAM arrays of larger size (e.g., 16-bit, 32-bit, and 64-bit memory blocks) can be explored for cache integration in modern SoCs.
- The design can be extended to sub-10 nm technology nodes, where device variability and leakage become more severe and require additional optimization techniques.
- Future work may incorporate advanced read/write assist schemes, voltage scaling methods, or adaptive biasing to support near-threshold computing and ultra-low-power operation.
- Integration with emerging transistor technologies such as GNRFET, CNTFET, or TFET may yield additional improvements in leakage control and operating frequency.

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