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An Area-Efficient AXI4-Lite SRAM Controller with SECDED Protection

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***Abstract*—** Memory controllers in safety-critical System-on-Chip (SoC) platforms must stay dependable even when stored bits are disturbed by radiation or electrical noise. This paper describes the design and functional verification of a soft-error-resilient SRAM controller that exposes an AMBA AXI4-Lite slave port. Where earlier parameterizable controllers concentrate on flexibility and burst throughput, the present design adds a Single Error Correction, Double Error Detection (SECDED) block based on the Hamming code, so that a corrupted word can be repaired before it reaches the bus master. The controller is written in SystemVerilog and exercised with a Universal Verification Methodology (UVM) testbench whose randomized fault-injection sequence flips memory bits on demand. Synthesis and implementation in Vivado for the Xilinx Zynq-7000 device (xc7z020) report 188 slice LUTs, 120 slice registers and 0.117 W of total on-chip power. Compared with a reference AXI4-Full reconfigurable controller (395 LUTs, 1.395 W), this is about 52% fewer LUTs and a 91.6% lower reported power figure. Simulation shows that every injected single-bit error is corrected and that double-bit errors raise an error flag, which makes the controller a suitable memory IP block for automotive and other safety-critical SoCs.

***Keywords*—** AXI4-Lite, SRAM controller, SECDED ECC, Hamming code, soft errors, fault injection, UVM, Zynq-7000, low-power VLSI.

I. Introduction

Automotive and industrial SoCs increasingly rely on compact, energy-efficient memory controllers that keep working under harsh operating conditions. SRAM is the usual choice for data buffers and control-register storage in such systems, and the AMBA AXI protocol is widely used to connect it to the rest of the chip [1]. As process geometries shrink, however, each SRAM cell holds less charge and becomes easier to upset. Electromagnetic interference and cosmic radiation can flip a stored bit without warning, and in a safety-critical function such a soft error may grow into a system failure.

A recent reconfigurable SRAM controller by Shaila et al. [2] is built around AXI4-Full. It supports wide parameter ranges but is aimed at high-bandwidth burst traffic, which costs extra logic and a larger power budget, and it offers no protection for the stored data. Many control-path uses need only one transfer per address, so the burst machinery is wasted area. Power can be reduced further by watching the memory control signals and gating the clock, or de-asserting chip enable, for idle memory [3].

This work therefore moves the controller to AXI4-Lite and adds a SECDED code derived from Hamming's construction [4]. The AXI4-Lite port brings the implementation down to 188 LUTs and the total on-chip power to 0.117 W, while the ECC logic corrects any single-bit upset in a stored word and flags double-bit upsets. Correct behavior is checked in a UVM environment [5] that includes a randomized fault-injection sequence. The main contributions are:

- an AXI4-Lite SRAM controller with configurable depth and width that embeds a SECDED encoder and decoder in its write and read paths;
- a UVM testbench with randomized fault injection that exercises both single-error correction and double-error detection;
- a post-implementation evaluation on Zynq-7000 together with a tabular comparison against a reference AXI4-Full controller.

II. Related Work

Shaila et al. [2] proposed a reconfigurable SRAM controller based on AXI4-Full in which memory depth and data width can be parameterized up to 1024 bits. Its implementation occupies 395 slice LUTs and reports a total power of 1.395 W, a cost that is hard to justify when the traffic never needs bursts.

AXI4-Lite is a reduced subset of the AXI specification intended for low-throughput peripherals where one data beat per address is enough [6]. On the verification side, Raj and Kumar [5] applied UVM to check protocol compliance of AXI-Lite peripheral controllers. UVM is a solid framework for functional verification, yet many reported environments do not automate fault injection, so the tolerance of the hardware to run-time data corruption is left untested [7]. FSM-based SRAM controllers have also been proposed to cure timing problems such as bus write contention and too-short pulse widths at 100 MHz operation [8].

The present work closes these gaps by combining AXI4-Lite signaling, integrated SECDED protection and a UVM fault-injection sequence. The result is a smaller, lower-power

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controller whose single-error correction is verified, aimed at automotive SoCs.

III. Controller Architecture

A. Reconfigurable Datapath and AXI4-Lite Interface

Fig. 1 shows the functional blocks of the proposed controller and its external signals. The AXI4-Lite master (the SoC) communicates with a slave interface that implements the handshake of the five independent channels (AW, W, B, AR and R), each governed by a VALID/READY pair [1]. Behind the interface sit a control FSM with an address decoder, which sequences every transaction and steers write data to the ECC encoder and read data back from the ECC decoder. The SRAM array stores each data word together with its parity bits, and its depth and width are configurable, so the controller can be adapted to different peripheral requirements without redesigning the RTL. The memory is described in SystemVerilog [9] and targeted at the Xilinx Zynq-7000 xc7z020 device. Because no burst logic is present, switching activity during transfers is lower, which helps keep the power consumption small.

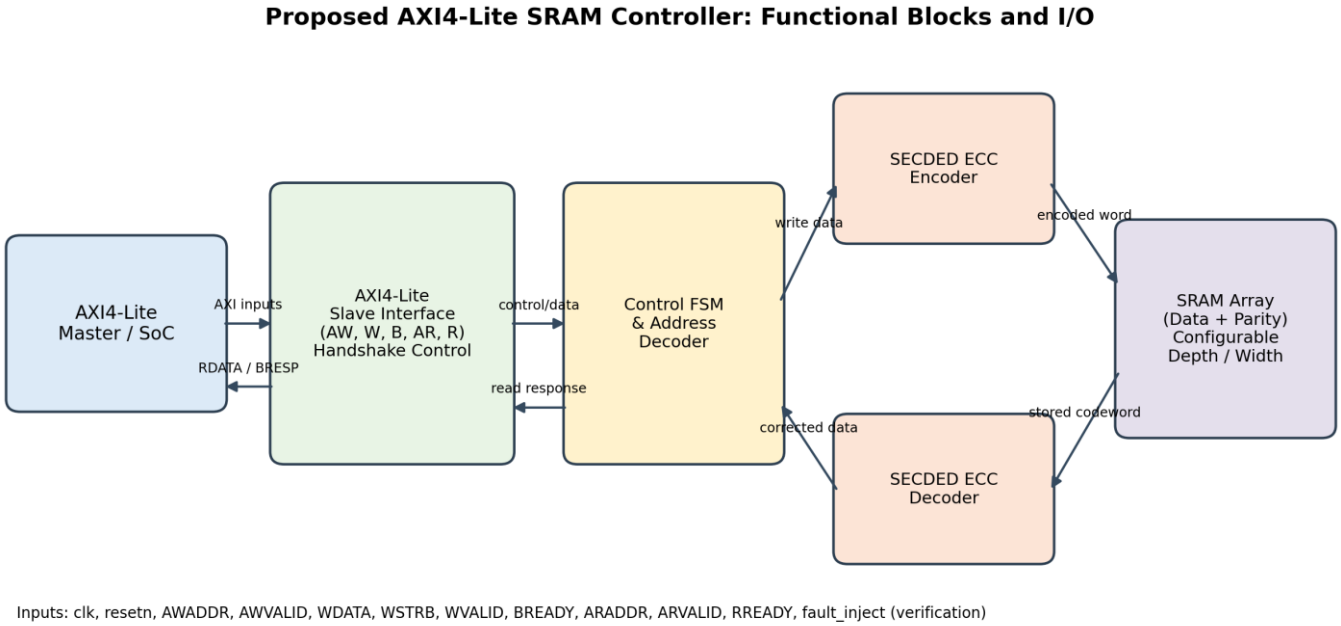


Fig. 1 Functional blocks and I/O of the proposed AXI4-Lite SRAM controller with SECDED ECC.

The controller inputs are clk, resetn, AWADDR, AWVALID, WDATA, WSTRB, WVALID, BREADY, ARADDR, ARVALID and RREADY, plus a fault-injection input used only during verification. Its outputs are AWREADY, WREADY, BRESP, BVALID, ARREADY, RDATA, RRESP, RVALID and the ECC single- and double-error flags. The RTL view produced by synthesis is given in Fig. 3.

B. SECDED ECC Protection

To protect stored data, a SECDED mechanism is placed between the AXI4-Lite interface and the SRAM array. It works in two phases.

1) Encoding (write path): when the master starts a write, the ECC encoder takes the incoming data and computes parity bits with the Hamming code algorithm [4]. The parity bits are appended to the data to form a codeword, and this codeword is what the SRAM stores. In this way each 32-bit input is tied to a fixed redundancy pattern, so integrity can be preserved even if radiation or interference later disturbs the cell.

2) Decoding (read path): on a read, the ECC decoder fetches the stored codeword and recomputes the parity to obtain a syndrome that reveals any bit flip incurred during storage. A single-bit error is corrected automatically before the data are returned to the master. A double-bit error cannot be repaired, so the controller instead raises an error flag to tell the host that the data are corrupted.

C. FSM-Based Control Flow

The operation of the controller is sequenced by a finite state machine, whose flow is summarized in Fig. 2. The FSM waits in IDLE until a valid transaction appears. A write passes through WRITE ACCEPT (AWVALID and WVALID handshake), ECC ENCODE (parity generation), SRAM WRITE (storage of the protected word) and WRITE RESPONSE (BVALID and BRESP). A read passes through READ ACCEPT (ARVALID handshake), SRAM READ (codeword fetch), ECC DECODE (syndrome and error check) and READ RESPONSE (RDATA, RVALID and RRESP). Once the response is accepted, the machine goes back to IDLE and waits for the next transaction.

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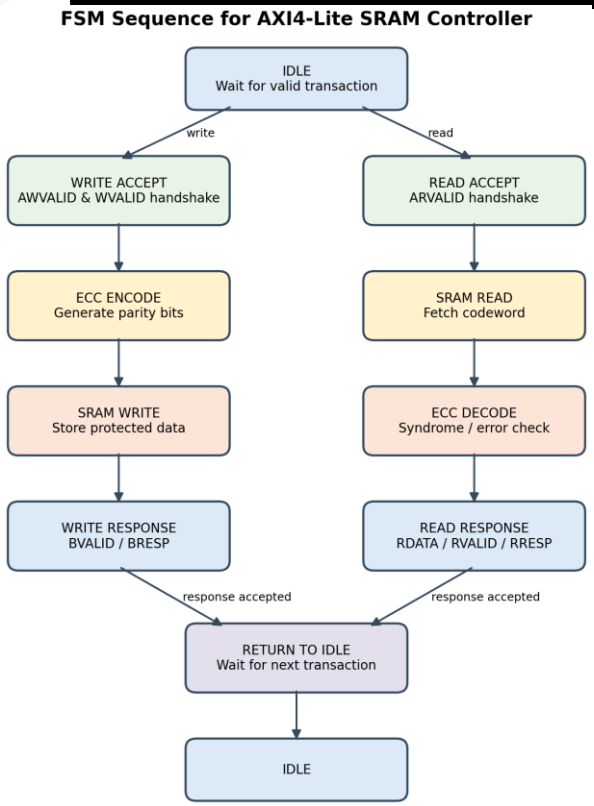


Fig. 2 FSM sequence of the AXI4-Lite SRAM controller for write and read transactions.

Several properties follow from this organization. First, parity generation and checking occupy dedicated ECC states, so they proceed in step with the AXI4-Lite handshakes. Second, the FSM watches the write-valid and read-valid inputs to leave IDLE for the matching write or read sequence. Third, AWREADY and WREADY are granted only after ECC encoding has finished, so that nothing but protected data reaches the memory array. Fourth, the return-to-IDLE step lets the data bus settle and the control strobes de-assert before the transfer direction changes, which plays the role of a precharge interval [8]. This compact structure is what allows the design to fit into only 188 slice LUTs.

IV. Verification Approach

Functional verification was carried out in a UVM environment [10]. To test the dependability of the ECC logic, a randomized fault-injection mechanism [7] was added to the testbench; it flips single bits of the data held in memory during write cycles, so that the decoder has to deal with genuine corruption on subsequent reads. Corrected read data and the raised error flags are then examined in simulation. The injection input appears as inject_error and the single-error flag as single_error in the waveform of Fig. 6.

V. Results and Discussion

The controller was synthesized and implemented with the Xilinx Vivado Design Suite for the Zynq-7000 xc7z020clg400-1 device. The reports show clear gains in both resource usage and power relative to conventional reconfigurable designs.

A. Resource Utilization

Hardware cost was measured as the number of look-up tables (LUTs) and flip-flops used on the FPGA. As Table I shows, the controller needs 188 slice LUTs and 120 slice registers. The reference AXI4-Full controller uses 395 LUTs, so the proposed design is about 52% smaller. The synthesized RTL structure and the placed LUT and register interconnections are shown in Fig. 3 and Fig. 4. This small footprint leaves room for the SECDED logic without straining a low-cost FPGA.

TABLE I
FPGA Resource Utilization for xc7z020clg400-1

Resource	Used	Available	Util. (%)
Slice LUTs	188	53,200	<1
Slice registers	120	106,400	<1
F7 muxes	78	26,600	<1
F8 muxes	39	13,300	<1
Bonded IOB	74	125	59

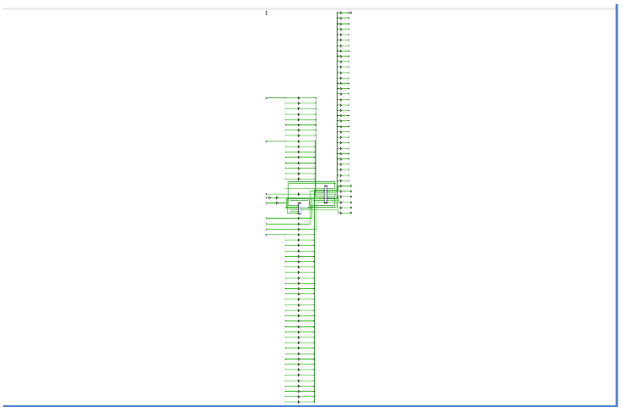


Fig. 3 Synthesized RTL schematic of the SRAM controller on Zynq-7000.

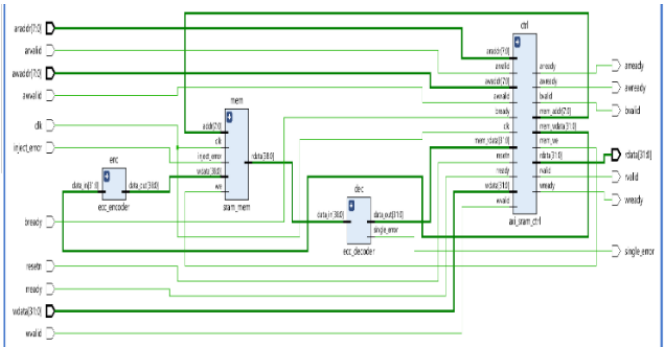


Fig. 4 Hardware schematic showing LUT and register interconnections.

B. Power Analysis

A main goal was to keep the power footprint of the controller small for automotive SoC use. The post-implementation power report from Vivado (Fig. 5) gives a total on-chip power of 0.117 W. Of this, 0.013 W (11%) is dynamic

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and 0.105 W (89%) is device static power. Within the dynamic part, clocks take 0.001 W, signals 0.002 W, logic less than 0.001 W and I/O 0.009 W. The junction temperature is 26.4 °C with a thermal margin of 58.6 °C (4.9 W) at 25 °C ambient. The low figure is attributed to replacing the complex AXI4-Full protocol with the lean AXI4-Lite protocol, which removes unnecessary switching during data transfers.

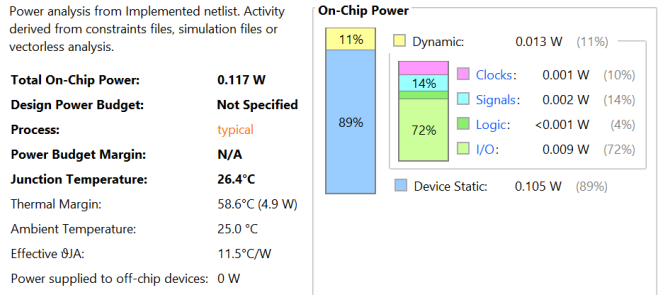


Fig. 5 Post-implementation power analysis report from Vivado.

C. Fault Tolerance Verification

The waveforms in Fig. 6 come from the UVM simulation with random single-bit faults injected during memory writes. The ECC decoder corrected every injected single-bit error, so the data returned on the read channel were always intact. Double-bit errors were detected and the corresponding error flag was raised, as the design specification requires.



Fig. 6 UVM simulation waveforms showing correction of injected single-bit errors.

D. Comparison with the Reference Design

The proposed AXI4-Lite controller with ECC is compared with the AXI4-Full reconfigurable controller of Shaila et al. [2], which was implemented on the same xc7z020 device family. The reference values are taken from the utilization and power reports published in [2]. Table II compares resources, Table III compares power and thermal figures, and Table IV compares functional features.

TABLE II
RESOURCE COMPARISON WITH REFERENCE [2]

Resource	Reference [2] (AXI4-Full)	Proposed (AXI4-Lite + ECC)	Change
Slice LUTs	395	188	−52.4%
Slice registers	603	120	−80.1%
LUT utilization (of 53,200)	<1%	<1%	—

TABLE III
POWER AND THERMAL COMPARISON WITH REFERENCE [2]

Metric	Reference [2] (AXI4-Full)	Proposed (AXI4-Lite + ECC)	Change
Total on-chip power	1.395 W	0.117 W	−91.6%
Dynamic power	1.261 W (90%)	0.013 W (11%)	−99.0%
Device static power	0.134 W (10%)	0.105 W (89%)	−21.6%
Clocks	0.003 W	0.001 W	—
Signals	0.002 W	0.002 W	—
Logic	0.001 W	<0.001 W	—
I/O	not listed	0.009 W	—
PS7 block	1.256 W	not listed	—
Junction temperature	41.1 °C	26.4 °C	−14.7 °C
Thermal margin	43.9 °C (3.7 W)	58.6 °C (4.9 W)	+14.7 °C

TABLE IV
FUNCTIONAL COMPARISON WITH REFERENCE [2]

Aspect	Reference [2]	Proposed
Bus protocol	AXI4-Full (burst capable)	AXI4-Lite (single beat)
Error protection	Not integrated	SECDED (Hamming code)
Fault injection	Not reported	Randomized, UVM-based
Verification result	Scoreboard: 10 writes and 10 reads matched	100% of injected single-bit errors corrected; double-bit errors flagged
Parameter range	Data and address width up to 1024 bits; FIFO depth 8 or 16	Configurable depth and width (32-bit data path reported)
Throughput	Write 16 beats/16 cycles; read 16 beats/17 cycles	Not evaluated in this work
Target device	XC7Z020-1CLG400C (PYNQ-Z2)	xc7z020clg400-1
Demonstration	Simulation and PYNQ-Z2 board	Simulation and post-implementation reports

The comparison shows that the proposed controller needs less than half of the LUTs and about one fifth of the registers of the reference design, and that its reported total power is lower by 91.6%. Two points should be kept in mind when reading these figures. First, the reference power report assigns 1.256 W to the Zynq processing-system (PS7) block, whereas the report for the proposed controller lists no such block, so the totals are not strictly like-for-like. Second, the reference controller supports bursts and widths up to 1024 bits, while the

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proposed controller is aimed at single-beat control-path traffic and its throughput was not measured. In return, the proposed design is the only one of the two that protects stored data against soft errors.

VI. Conclusion

This paper presented the design, implementation and functional verification of a fault-tolerant, reconfigurable SRAM controller with an AMBA AXI4-Lite interface. The work addresses the trade-off between hardware complexity and data reliability in automotive SoC environments. Moving from AXI4-Full to AXI4-Lite cut the implementation to 188 slice LUTs, and the SECDED ECC logic guarantees recovery of all single-bit soft errors, which was demonstrated through randomized fault injection in a UVM environment. Implementation on the Xilinx Zynq-7000 gave a total on-chip power of 0.117 W, a substantial improvement over existing reconfigurable memory controllers. Together with a 91.6% lower reported power, this low area and integrated fault tolerance make the controller a good IP core for safety-critical automotive SoC architectures.

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