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A Comparison Review on Quaternary Logic Gates

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***Abstract*—Significant issues including higher power consumption, leakage currents, and connectivity complexity in contemporary VLSI systems have been brought about by the ongoing scaling of CMOS technology. By increasing information density and lower connection overhead, Multi-Valued Logic (MVL) has a become a viable substitute to get around these restrictions. Quaternary logic offers an effective trade-off between circuit complexity and performance among different MVL systems. Because of its superior electrical characteristics, such as high carrier mobility, near-ballistic transport, and the capacity to create multiple threshold voltage, carbon nanotube field effect transistor (CNTFET) technology has attracted a lot of interest for the implementation of quaternary logic circuits. Quaternary logic gates, including inverters, NAND, and NOR circuits, can be efficiently realized because to them. A thorough analysis of CNTFET-based quaternary logic gate design is presented in this study, with an emphasis on implementation strategies, performance assessment, and comparison with traditional methods. Additionally, it is noted that whereas quaternary logic gates and arithmetic circuits like adders this gap emphasizes the need for more study to create effective quaternary subtractors based on CNTFETs for next generation low-power VLSI application.**

***Keywords*—CNTFET, Quaternary Logic, Multi-Valued Logic, VLSI, Low Power, Nanoelectronics.**

I. INTRODUCTION

The need for high speed, low-power, and area-efficient digital systems has grown dramatically due to the quick development of very large-scale integration (VLSI) technology. Despite their widespread use, conventional binary logic circuits encounter a number of difficulties at deep nanoscale levels, such as higher power dissipation, connectivity complexity, and leakage currents [1], [2]. These restrictions prevent contemporary integrated circuits from achieving even performance gains. Multi-valued logic (MVL) has become a viable substitute for conventional binary systems in order to overcome these difficulties, MVL systems use many discrete logic levels to increase information density and decrease the number of interconnections, in contrast to binary logic, which uses two levels to represent information [3]-[5]. Quaternary logic, which functions with four logic levels (0,1,2, and 3), offers an efficient trade-off between circuits complexity and computing performance among several MVL schemes [6]. However, problems including threshold voltage changes, decreased noise margins, and increased leakage current make it challenging to design dependable multi-valued logic circuits using conventional CMOS technology [7]. Carbon Nanotube Field Effect Transistors (CNTFETs) have become a viable substitute for nanoscale circuit design in this regard. High carrier mobility, near- ballistic transport, and enhanced electrostatic control are just a few of the superior electrical properties that CNTFETs provide [8], [9]. More significantly, by varying the diameter and chirality of carbon nanotubes, the threshold voltage of CNTFETs may be accurately adjusted, making it possible to efficiently realize the numerous logic levels needed for quaternary logic systems [10].

The basic building blocks for creating intricate arithmetic and logic units in MVL system are quaternary logic gates, which include inverters, NAND, and NOR circuits. The design and optimization of CNTFET based quaternary logic gates and arithmetic circuits, including adders and multipliers, have been the subject of numerous studies, which have shown improvements in power consumption, latency, and overall performance [11]-[13]. Despite these developments, quaternary subtractor circuit design and implementation have received less attention than other arithmetic units. A major research gap in the creation of comprehensive quaternary arithmetic systems in highlighted by the absence of effective subtractor architectures. Therefore, optimized CNTFET-based quaternary subtractor designs for next generation low-power and high-performance VLSI applications need more research.

II. FUNDAMENTALS OF QUATERNARY LOGIC GATES

By combining more than two discrete logic levels to describe information, Multi-Valued Logic (MVL) has become an effective substitute for traditional binary logic. Quaternary logic is one of the most popular MVL systems because it can provide increased information density while lowering connectivity complexity [1], [3]. Voltage levels 0, VDD/3, 2VDD/3, and VDD, respectively, are commonly used to representation makes compact circuit design and effective data processing possible. Devices that can support several stable threshold voltage levels are necessary for the implementation of quaternary logic circuits. When used to multi-valued logic devices, conventional CMOS technology encounters difficulties like decreased noise margins and

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greater leakage currents [2]. On the other hand, because they can support numerous threshold voltages by varying the diameter of carbon nanotubes, Carbon Nanotube Field Effect Transistors (CNTFETs) offer an efficient alternative. Quaternary logic levels can be accurately implemented with better performance and lower consumption because to this special feature [1], [4].

Table 1. Quaternary logic levels and corresponding voltages [3]

Logic Level	Voltage Level
0	0
1	VDD/3
2	2VDD/3
3	VDD

III. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

A number of issues, including short-channel effects, higher leakage current, and decreased gate control, have surfaced as traditional CMOS technology gets closer to its scaling limits, restricting its performance in nanoscale VLSI design [2]. Because of its better electrical and physical characteristics, Carbon Nanotube Field Effect Transistors (CNTFETs) have been presented as a viable substitute to get over these restrictions. Like a traditional MOSFET, a CNTFET uses a semiconducting carbon nanotube as the channel material between the source and drain terminals. It is composed of a gate electrode, source, drain, and gate dielectric. The applied gate voltage regulates the current conduction. Carrier transport in CNTFETs is almost ballistic because of the one-dimensional structure of carbon nanotubes, which leads to high-speed operation and lower power consumption [4].

Schottky Barrier CNTFETs and MOSFET-like CNTFETs are the two main categories of CNTFETs. Because of their superior switching properties and reduced contact resistance, MOSFET-like CNTFETs are frequently utilized in digital circuit applications. The capacity of CNTFET technology to achieve numerous threshold voltages by changing the carbon nanotube's diameter is one of its most important benefits. Quaternary logic and other multi-valued logic systems can be implemented effectively since the threshold voltage is inversely related to the nanotube diameter [5]

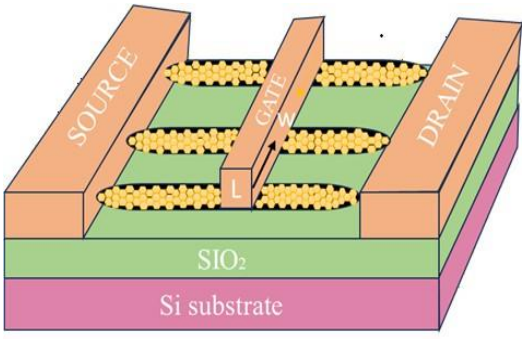

Fig. 1. CNTFET structure

IV. LITERATURE SURVEY

The design of quaternary logic gates employing CNTFET technology has been the subject of extensive research in recent years, with an emphasis on enhancing circuit complexity, speed, and power efficiency. To implement basic arithmetic circuits and logic gates in multi-valued logic systems, several methods have been put forth. A CNTFET-based quaternary inverter design utilizing multi-threshold voltage approaches was presented in [1]. Accurate voltage representation for quaternary logic is made possible by the design's use of various carbon nanotube diameters to achieve numerous logic levels. When compared to traditional CMOS-based designs, the suggested inverter showed faster switching and lower power usage. CNTFET technology was used to offer optimal designs of quaternary NAND and NOR gates in [2].

Effective multi-level processing was made possible by the circuits' foundation in minimum and maximum logic operations. The suggested architecture produced reduced latency and enhanced performance because of the near-ballistic transport characteristics of CNTFETs. A thorough process for creating quaternary logic circuits based on CNTFETs was presented in [3]. The study focused on threshold voltage management for stable multi-level operation and includes implementations of inverters and simple gates. When compared to binary logic circuits, simulation results shown notable improvements in power-delay product.

Using CNTFET technology, a low-power quaternary arithmetic circuit was proposed in [4], with a primary focus on quaternary adder design. The design increased computing efficiency and decreased the number of transistors. Nevertheless, adding operations were the primary focus of the effort; subtraction capabilities was not taken into account. A high-performance CNTFET-based multi-valued logic system that incorporates quaternary logic gates into arithmetic units was introduced in [5]. The design showed decreased interconnection complexity and increased scalability. Quaternary subtractor circuit implementation is still mainly unexplored despite these developments.

It is clear from the description above that the majority of current research focuses on arithmetic circuits like adders and quaternary logic gates. However, there hasn't been much study done on CNTFET-based quaternary subtractor design. This draws attention to a substantial research need and encourages more investigation into creating effective quaternary subtractor circuits for upcoming VLSI applications.

Table 2. comparison of CNTFET-based quaternary logic design

Ref	Circuit type	power	delay	Key contribution
[1]	inverter	Low	Fast	Multi-threshold design
[2]	NAND/NOR	Low	Very fast	Efficient MVL logic
[3]	Logic Gates	Moderate	Fast	Improved PDP

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[4]	Adder	Low	Fast	Reduced transistor count
[5]	MVL system	Very low	Very fast	Scalable architecture

V. QUATERNARY LOGIC GATES DESIGN

the implementation of arithmetic and logic operations depends heavily on quaternary logic gates, which are essential parts of multi-valued logic systems. Compared to binary logic systems, these gates four discrete logic levels (0, 1, 2, and 3) allow for greater information density and simpler interconnections. Utilizing Carbon Nanotube Field Effect Transistor (CNTFET) technology to construct quaternary logic gates has several benefits, including increased scalability, reduced power consumption, and fast operation. Quaternary logic systems benefit greatly from CNTFETs ability to precisely generate and regulate several logic levels due to their multi-threshold voltage capabilities [5], [10].

A. Quaternary Inverters

Because they produce the complementary logic levels needed for additional processing, quaternary inverters are crucial components of multi-valued logic system. Quaternary inverters are categorized as positive ternary inverters (PTI), negative ternary inverters (NTI), standard quaternary inverters (SQI), and intermediate quaternary inverters (IQI) according to their voltage transfer characteristics [5], [14]. To accomplish precise mapping between input and output logic levels, the suggested inverter circuits make use of CNTFET devices with various threshold voltages. Multiple switching thresholds are established by varying the carbon nanotube width, guaranteeing accurate voltage transitions between quaternary levels.

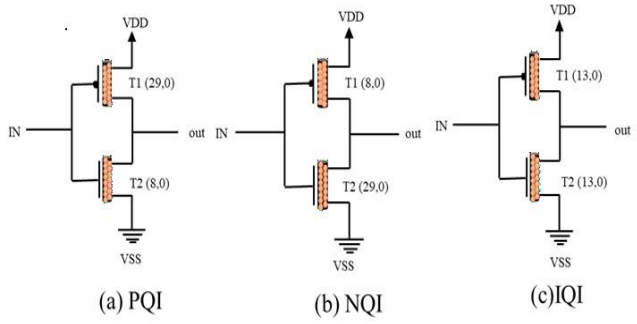

Fig. 2. Quaternary inverters circuits [20]

B. Standard quaternary inverter (SQI)

The Standard Quaternary Inverter (SQI) is one of the fundamental inverter structures in multi-valued logic systems. The input logic levels are completely inverted, mapping the highest input level to the lowest output level and vice versa. relationship: Several CNTFET devices with various threshold voltages are used to implement SQI using CNTFET technology. Different switching thresholds are produced by varying the diameter of carbon nanotubes, enabling precise mapping of input voltage levels to matching output values [5], [10]. The SQI circuit ensures dependable operation without intermediate undefined states by displaying well-defined voltage transfer characteristics with abrupt transitions between logic levels. Due to the near-ballistic transport and high carrier mobility of CNTFETs, the SQI provides improved performance in terms of speed and power efficiency compared to conventional CMOS-based designs.

Moreover, SQI is a crucial part of multi-valued logic system design since it is a basic building block for creating intricate quaternary logic circuits like NAND, NOR, and arithmetic units [14].

C. Quaternary NAND gate (SQNAND)

The minimal logic operation, in which the output equals the minimum of the input logic levels, provides the basis for the implementation of the quaternary NAND gate. CNTFET devices are used in the SQNAND circuit to identify and transmit the lowest input voltage level to the output [5], [9].

To provide appropriate logic level transitions and signal processing, the circuit uses inverter stages like IQI. The SQNAND circuit achieves fast switching and low power consumption because of the near-ballistic transport characteristics of CNTFETs. Reliability in multi-valued logic systems is ensured by the circuit's transient response, which shows precise transitions between quaternary logic levels (0–3) without distortion or undefined states [16].

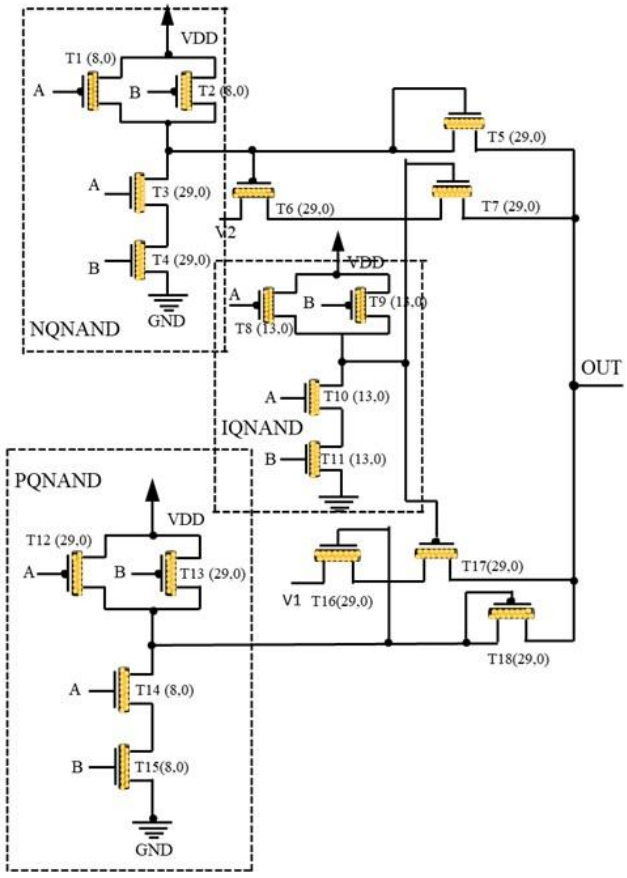

Fig. 3. Quaternary SQNAND circuit [20]

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D. Quaternary NOR gate

A key logic gate in multi-valued logic systems, the quaternary NOR gate is based on the maximal logic operation. The largest value among the input logic levels in this gate is represented by the output. Effective multi-level signal processing is made possible by the NOR operation, which generates an output that reflects the highest input level for quaternary inputs between 0 and 3 [5]. Several transistors with various threshold voltages are used to build the quaternary NOR gate utilizing CNTFET technology. The diameter of carbon nanotubes can be changed to manage these threshold voltages, enabling accurate input voltage level sensing. In order to ensure proper logical operation, the circuit is set up so that the highest input voltage dominates the output [6], [10].

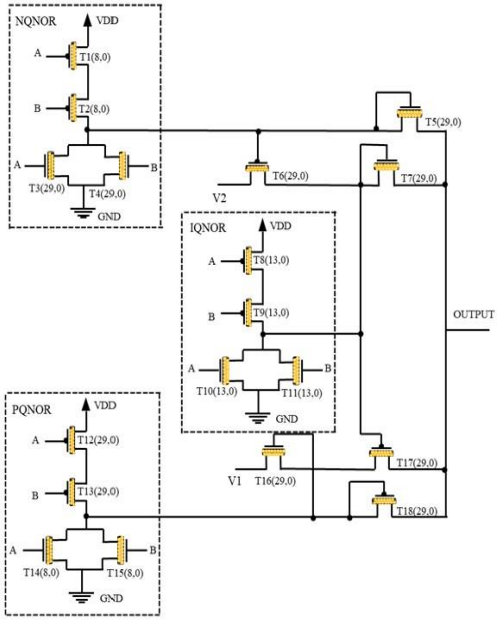


Fig. 4. Quaternary SQNOR circuit [20]

VI. PERFORMANCE COMPARISON OF QUATERNARY LOGIC GATES

Table 3. performance evaluation of SQI [20]

Ref	Pavg {µw)	Tpd (Ps)	PDP	EDP
SQI-1- [21]	511.10	4.886	2.499	12.215
SQI-2- [22]	315.63	8.217	21.312	21.312
SQI-3- [23]	97.983	9.088	7.052	7.052
SQI-4- [24]	176.96	7.710	10.699	10.699
SQI-5- [25]	36.034	9.373	3.165	3.165
SQI-6 used for ALU - [20]	31.446	7.948	0.249	1.986

Table 4. performance evaluation of SQNAND [20]

Ref	Pavg {µw)	Tpd (Ps)	PDP	EDP
SQNAND-1- [22]	431.13	5.211	2.247	11.711
SQNAND-2- [23]	331.50	7.695	2.633	20.915
SQNAND-3- [24]	363.69	7.695	2.798	21.535
SQNAND-4- [25]	116.97	16.831	1.968	33.136
SQNAND-used in ALU- [20]	54.557	10.945	0.597	6.535

Table 5. Performance evaluation of SQNOR [20]

Ref	Pavg (µw)	Tpd (Ps)	PDP	EDP
SQNOR-1- [22]	541.88	5.415	2.934	15.892
SQNOR-2- [23]	437.55	12.044	5.270	63.475
SQNOR-3- [24]	413.56	7.817	3.232	25.271
SQNOR-4- [25]	42.510	15.566	0.661	10.30
SQNOR-used in ALU- [20]	9.476	10.507	0.562	1.046

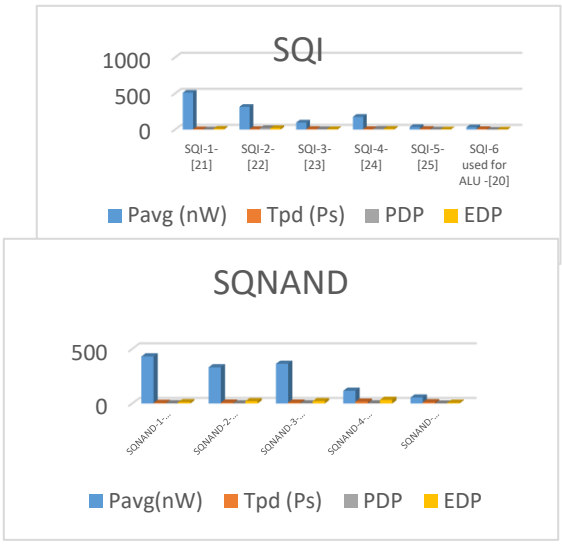


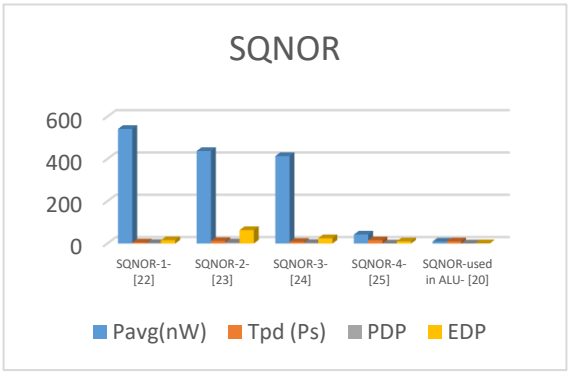
Fig. 5. SQI performance evaluation graph [20]

FIG. 6. SQNAND PERFORMANCE EVALUATION GRAPH [20]

Fig. 7. SQNOR performance evaluation graph [20]

VII. FUTURE SCOPE

Significant research has been done on the design of basic logic gates and arithmetic units like adders and multipliers, according to the assessment of CNTFET-based quaternary logic circuits. Nonetheless, there is still a dearth of research on quaternary subtractor circuit design and implementation. A quaternary subtractor is a crucial part of sophisticated processing units and full multi-valued arithmetic systems.



A significant research gap in the field of quaternary logic design is highlighted by the lack of effective subtractor are. Biotectures. Thus, CNTFET-based quaternary subtractor circuits with optimal performance in terms of power consumption, delay, and circuit complexity can be the subject of future research. The accuracy and stability of logic levels

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can be further enhanced by the application of multi-threshold CNTFET technology, allowing for effective subtraction operations in multi-valued logic systems. Furthermore, the practical application of CNTFET-based quaternary circuits in nanoscale VLSI systems can be improved by additional developments in fabrication and integration techniques.

VIII. CONCLUSION

A thorough analysis of CNTFET-based quaternary logic gates for multi-valued VLSI applications was provided in this research. The study included the design of important logic gates, such as inverters, NAND, and NOR circuits, as well as the principles of quaternary logic and the benefits of CNTFET technology.

When compared to traditional methods, a thorough performance evaluation of several quaternary logic gates showed gains in power efficiency, propagation latency, and overall circuit performance. The findings demonstrate the great suitability of CNTFET-based designs for the implementation of effective multi-valued logic systems. Additionally, as the majority of current research focuses on logic gates and adders, the study found a substantial research gap in the design of quaternary subtractor circuits. The creation of comprehensive and high-performing arithmetic systems may result from filling this gap. All things considered, CNTFET-based quaternary logic offers advantages in speed, power efficiency, and scalability, making it a promising path for future nanoscale VLSI design.

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